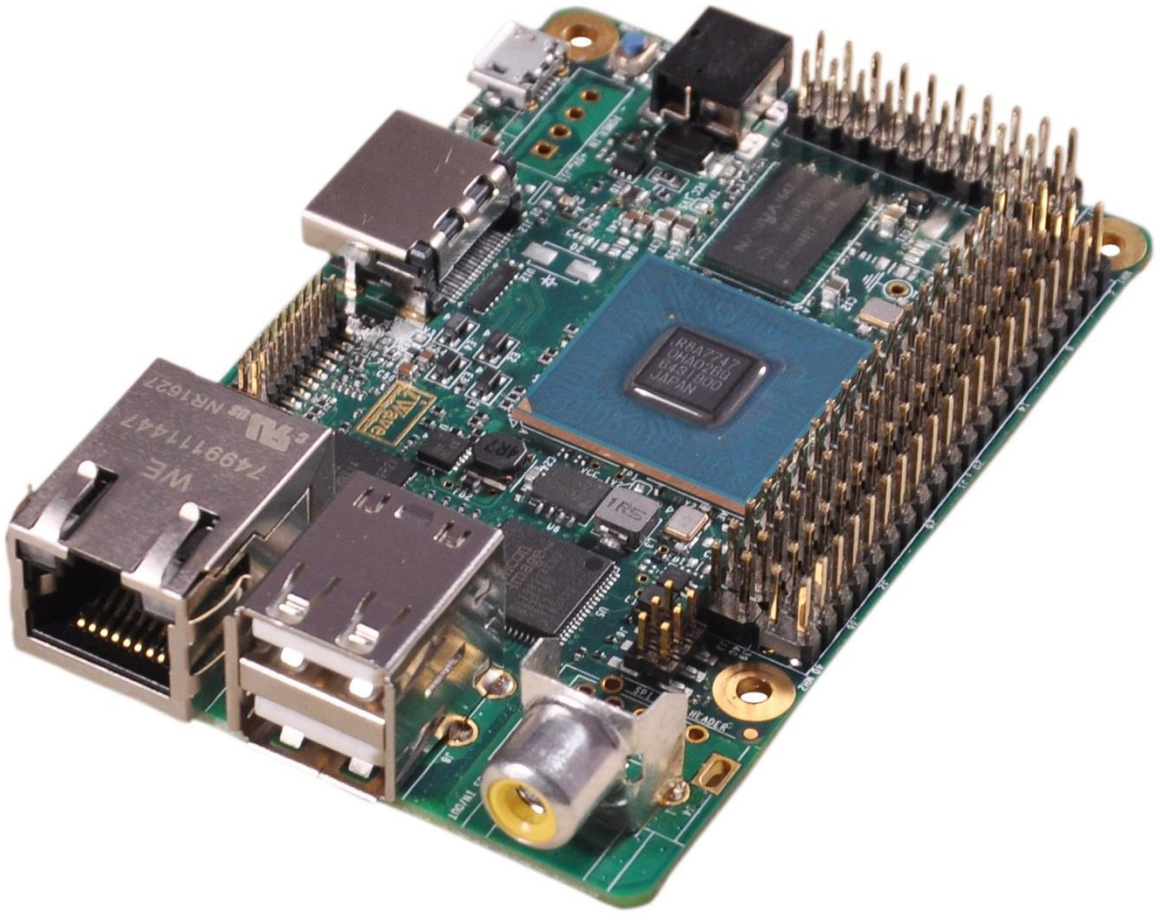
iW-RainboW-G23S
RZ/G1C Single Board Computer
Hardware User Guide



iWave
Embedding Intelligence

Document Revision History

Document Number		iW-PRFCC-UM-01-R3.0-REL1.0-Hardware
Revision	**Date**	**Description**
1.0	18th Aug 2017	Initial Release Version

PROPRIETARY NOTICE: This document contains proprietary material for the sole use of the intended recipient(s). Do not read this document if you are not the intended recipient. Any review, use, distribution or disclosure by others is strictly prohibited. If you are not the intended recipient (or authorized to receive for the recipient), you are hereby notified that any disclosure, copying distribution or use of any of the information contained within this document is STRICTLY PROHIBITED. Thank you. "iWave Systems Tech. Pvt. Ltd."

Disclaimer

iWave Systems reserves the right to change details in this publication including but not limited to any Product specification without notice.

No warranty of accuracy is given concerning the contents of the information contained in this publication. To the extent permitted by law no liability (including liability to any person by reason of negligence) will be accepted by iWave Systems, its subsidiaries or employees for any direct or indirect loss or damage caused by omissions from or inaccuracies in this document.

CPU and other major components used in this product may have several silicon errata associated with it. Under no circumstances, iWave Systems shall be liable for the silicon errata and associated issues.

Trademarks

All registered trademarks, product names mentioned in this publication are the property of their respective owners and used for identification purposes only.

Certification

iWave Systems Technologies Pvt. Ltd. is an ISO 9001:2015 Certified Company.

Warranty & RMA

Warranty support for Hardware: 1 Year from iWave or iWave's EMS partner.
For warranty terms, go through the below web link,
http://www.iwavesystems.com/support/warranty.html

For Return Merchandise Authorization (RMA), go through the below web link,
http://www.iwavesystems.com/support/rma.html

Technical Support

iWave Systems technical support team is committed to provide the best possible support for our customers so that our Hardware and Software can be easily migrated and used.
For assistance, contact our Technical Support team at,

Email : support.ip@iwavesystems.com
Website : www.iwavesystems.com
Address : iWave Systems Technologies Pvt. Ltd.
7/B, 29th Main, BTM Layout 2nd Stage,
Bangalore, Karnataka,
India – 560076

Table of Contents

List of Figures

List of Tables

1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the RZ/G1C Single Board Computer based on the Renesas's RZ/G1C Application processor. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This guide provides detailed information on the overall design and usage of the RZ/G1C SBC from a Hardware Systems perspective.

1.2 Overview

The RZ/G1C Single Board Computer is an extension of RZ/G1C CPU. SBC is an off-the-shelf board that integrates all the core features of a common PC. RZ/G1C SBC has a form factor of 85mm x 56mm and provides the functional requirements for an embedded application.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BPP	Bits Per Pixel
BSP	Board Support Package
CAN	Controller Area Network
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CVBS	Composite Video Signal
DDR3	Double Data Rate 3
eMMC	Enhanced Multi Media Card
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
HSCIF	High Speed Serial Communication Interface with FIFO
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group
Kbps	Kilobits per second
LVDS	Low Voltage Differential Signalling
MAC	Media Access Controller
MB	Mega Byte
Mbps	Megabits per sec
MHz	Mega Hertz

Acronyms	Abbreviations
MSIOF	Clock-Synchronized Serial Interface with FIFO
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
QSPI	Quad Serial Peripheral Interface
SBC	Single Board Computer
SCIF	Serial Communication Interface with FIFO
SD	Secure Digital
SDHI	SD Card Host Interface
SSI	Serial Sound Interface
SDRAM	Synchronous Dynamic Random Access Memory
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go

1.4 Terminlogy Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
LVDS	Low Voltage Differential Signal
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SBC.

1.5 References

- RZ/G1C CPU Hardware User Manual

1.6 Important Note

In this document, wherever CPU signal name is mentioned, it is followed as per below format for easy understanding.

- If CPU pin has multiplexing option and selected particular function, then the signal name is mentioned as
  "Selected Function Name (GPIO Number)"
  Example: CAN0_RX_A(GP0_11)
  In this signal, ***CAN0_RX*** is the functionality which we are using and ***GP0_11*** is the GPIO number.

- If CPU pin has multiplexing option and selected as GPIO function, then the signal name is mentioned as
  "GPIO (GPIO Number)"
  Example: GPIO(GP4_8)
  In this signal, ***GPIO*** is MUX functionality which we are using and ***GP4_8*** is the GPIO number.

- If CPU pin doesn't have multiplexing option, then the signal name is mentioned as,
  "Function name"
  Example: TXOUT0M
  In this signal, functionality which we are using is LVDS ***TXOUT0M***

Note: The above naming is not applicable for other signals which are not connected to CPU.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the RZ/G1C SBC features and Hardware architecture with high level block diagram. Also, this section provides detailed information about SBC Expansion connectors pin assignment and usage.

2.1 RZ/G1C SBC Block Diagram

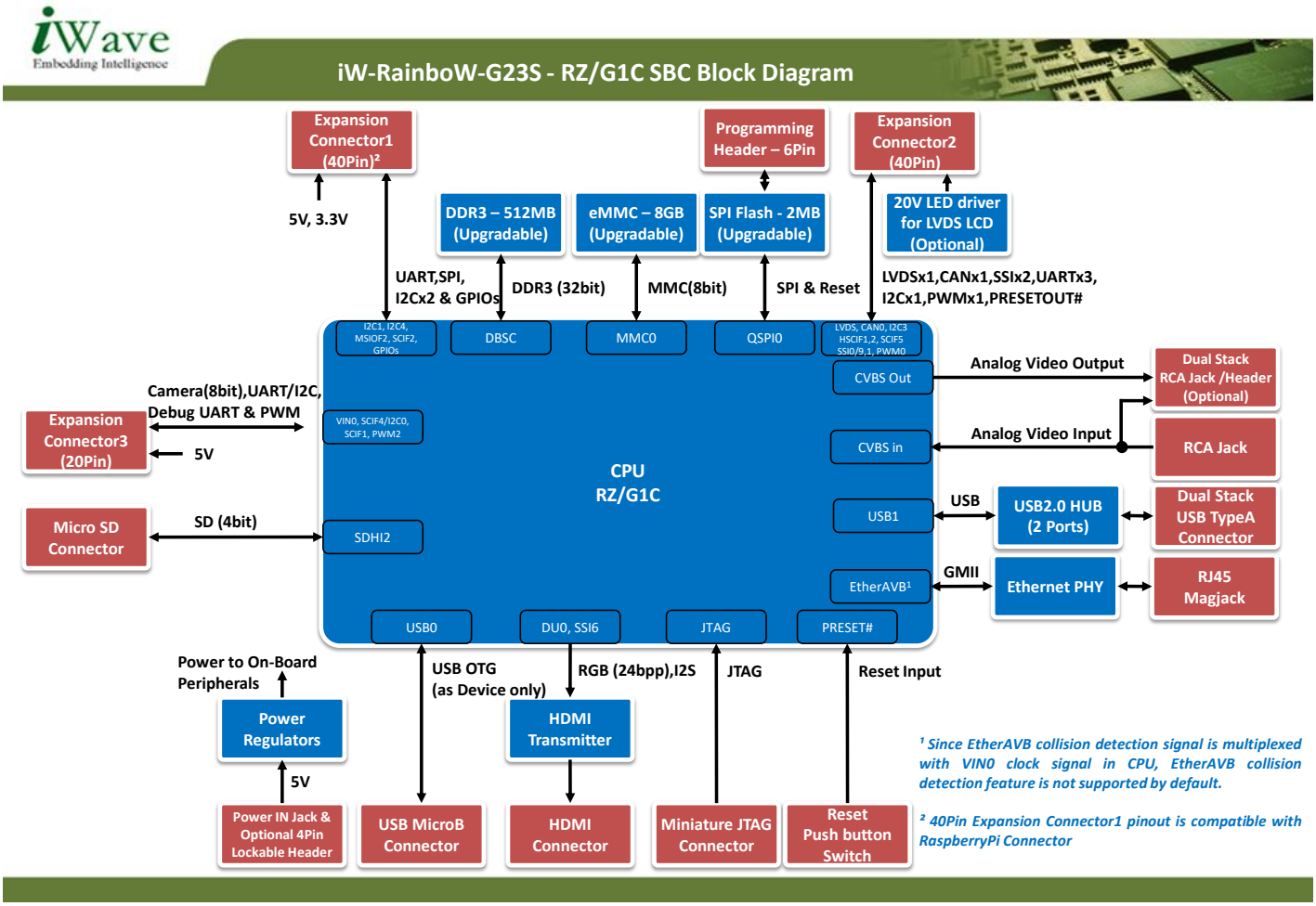


Figure 1: RZ/G1C SBC Block Diagram

2.2 RZ/G1C SBC Features

The RZ/G1C Single Board computer supports the following features.

CPU

- Renesas' RZ/G1C Dual/Solo ARM Cortex™-A7 MPCore™ cores @ 1GHz

Memory

- DDR3 SDRAM – 512 MB (Expandable Up to 2GB)
- SPI Flash - 2MB (Expandable)
- eMMC Flash - 8GB (Expandable)
- Micro SD Connector

Communication Features

- 100/1000Mbps Ethernet through RJ45 MagJack [1]
- USB2.0 Host x 2 Ports through Dual Stack TypeA Connector
- USB2.0 OTG as Device x 1 Port through MicroB Connector

Video Features

- HDMI x 1 Port through HDMI connector
- CVBS Video Input through RCA Jack [2]
- CVBS Video Output through RCA Jack/Header (Optional) [2]

Other Features

- JTAG Header
- SPI Flash Programming Header
- Reset Switch

Expansion Connector1 (40 Pin) Interfaces [3]

- Data UART (without CTS & RTS) x 1
- SPI x1
- I2C x 2
- GPIOs (17nos)

Expansion Connector2 (40 Pin) Interfaces

- LVDS x 1
- CAN x 1
- I2S Audio Interface (SSI) x 2
- DATA UART (with CTS & RTS) x 2
- DATA UART (without CTS & RTS) x 1
- I2C x 1
- PWM x 1

Expansion Connector3 (20 Pin) Interfaces

- Debug UART
- Data UART (without CTS & RTS)/I2C x 1
- Parallel Camera (VIN0 – 8bit) x 1 Port [1]
- PWM x 1

General Specification

- Power Input Jack**:** 5V,2.5A
- Power Input Lockable Header (Optional)
- Form Factor **:** 85mm x 56mm

[1] In RZ/G1C CPU, EtherAVB collision detection signal and VIN0 clock signal is multiplexed in same pin and so EtherAVB collision detection is not supported by default.

[2] RZ/G1C CPU supports one CVBS Video IN and one CVBS Video Out port. By default CVBS Video IN port is supported on RZ/G1C SBC. To support CVBS Video Out port, contact iWave.

[3] Expansion connector1 pinout is compatible with Raspberry Pi connector pinout.

2.3 RZ/G1C CPU

The RZ/G1C SBC is based on Renesas's RZ/G1C CPU with built-in Dual/Solo ARM Cortex®-A7 MPCore® which can operate up to 1 GHz/core. The Block Diagram of RZ/G1C CPU from Renesas's website is shown below for reference.

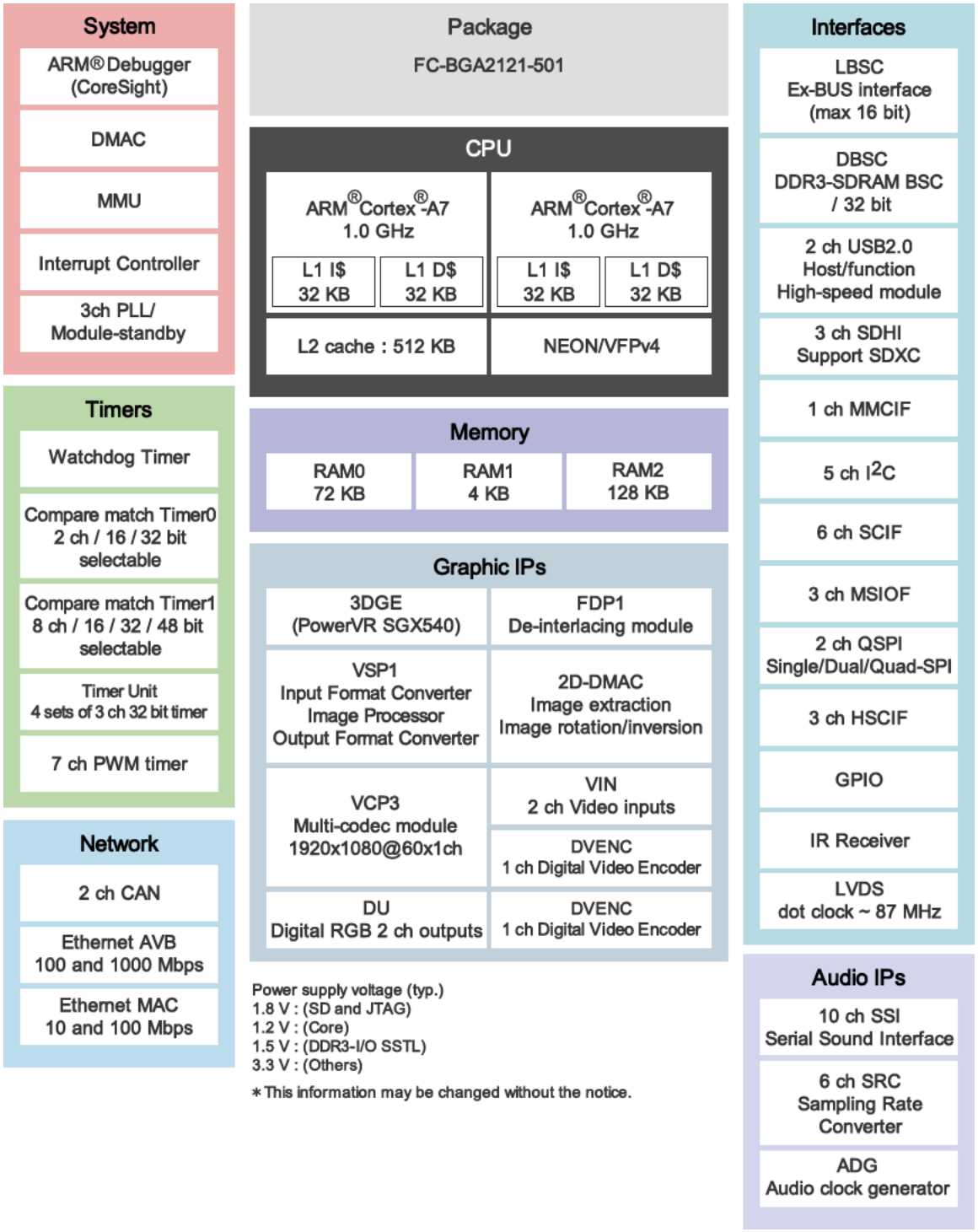


Figure 2: RZ/G1C CPU Simplified Block Diagram

Note: Please refer the latest RZ/G1C Hardware User Manual for more details which may be revised from time to time.

2.4 Memory

2.4.1 DDR3 SDRAM

The RZ/G1C SBC supports 512MB DDR3 RAM memory by default. This is connected to CPU's DBSC3 DDR3 controller in 32bit x 1ch mode where it uses two 256MB DDR3-SDRAM ICs. This device operates at 1.5V voltage level. DDR3-SDRAM ICs are physically located on either side of the SBC. The RAM size can be expandable up to maximum of 2GB.

2.4.2 SPI NOR Flash

The RZ/G1C SBC supports 2MB SPI NOR Flash as default boot device. This is connected to QSPI controller of the RZ/G1C CPU and operates at 3.3 Voltage level. While RZ/G1C booting, boot program in the on-chip ROM starts up the QSPI and SYS-DMAC channel 1, and transfers the loader program previously stored in the SPI Flash to the on-chip RAM via the QSPI controller. After loader program is transferred, the program automatically jumps to the top address of the loader program. The SPI flash memory is physically located on bottom side of the SBC.

To program the boot code in to the SPI flash for the first time, use JTAG debugger through JTAG Header (J13). Optionally the external SPI programmer through SPI Flash Programming Header (J6) (or) 8pin SOIC test clips (Example part: 923655-08 from 3M) can be used for programming the SPI flash.

2.4.3 eMMC Flash

The RZ/G1C SBC supports 8GB eMMC Flash memory as mass storage. eMMC is directly connected to the MMC0 controller of the RZ/G1C CPU which supports MMC 4.4.1 and operating at 3.3V Voltage level. The eMMC flash memory is physically located on bottom side of the SBC. The memory size of the eMMC Flash can be expandable.

2.4.4 Micro SD Connector

The RZ/G1C SBC supports Micro SD connector which can be used to connect Micro SD card as Mass storage. Micro SD card connector (J15) is directly connected to the SDHI2 controller of the RZ/G1C CPU. This supports default, high-speed and UHS-I/SDR50 transfer modes upto 78 MHz. It also supports card detect feature through RZ/G1C GPIO "GP4_20". The main power to Micro SD Card Connector is 3.3 Voltage.

The RZ/G1C SBC supports configurable IO voltage levels for SDHI2 lines which can be controlled through CPU GPIO GP2_24. If GP2_24 is set to low, then 1.8V IO level is selected for SDHI2 lines. If GP2_24 is set to high, then 3.3V IO level is selected for SDHI2 lines. Micro SD Connector is physically located on bottom side of the SBC as shown below.

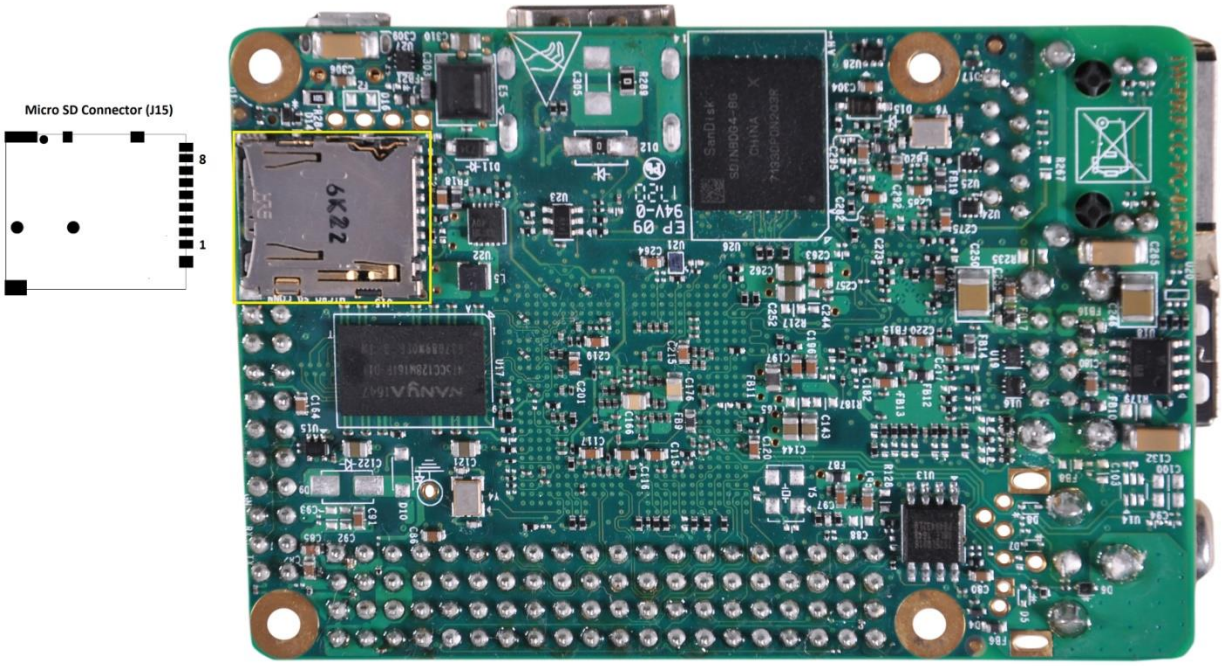


Figure 3: Micro SD Connector

2.5 Communication Features

2.5.1 100/1000Mbps Ethernet Port

The RZ/G1C SBC supports 100/1000Mbps Ethernet through RZ/G1C CPU's EtherAVB interface. The MAC is integrated in the RZ/G1C CPU and connected to the external Gigabit Ethernet PHY "KSZ9031MNX". The Gigabit Ethernet PHY output is directly to connected to RJ45 Magjack (J10).

RZ/G1C SBC also supports Activity (Yellow) and Link (Green) LED indications on RJ45 Magjack. The 100/1000Mbps Ethernet Connector is physically located on top side of the SBC as shown below.

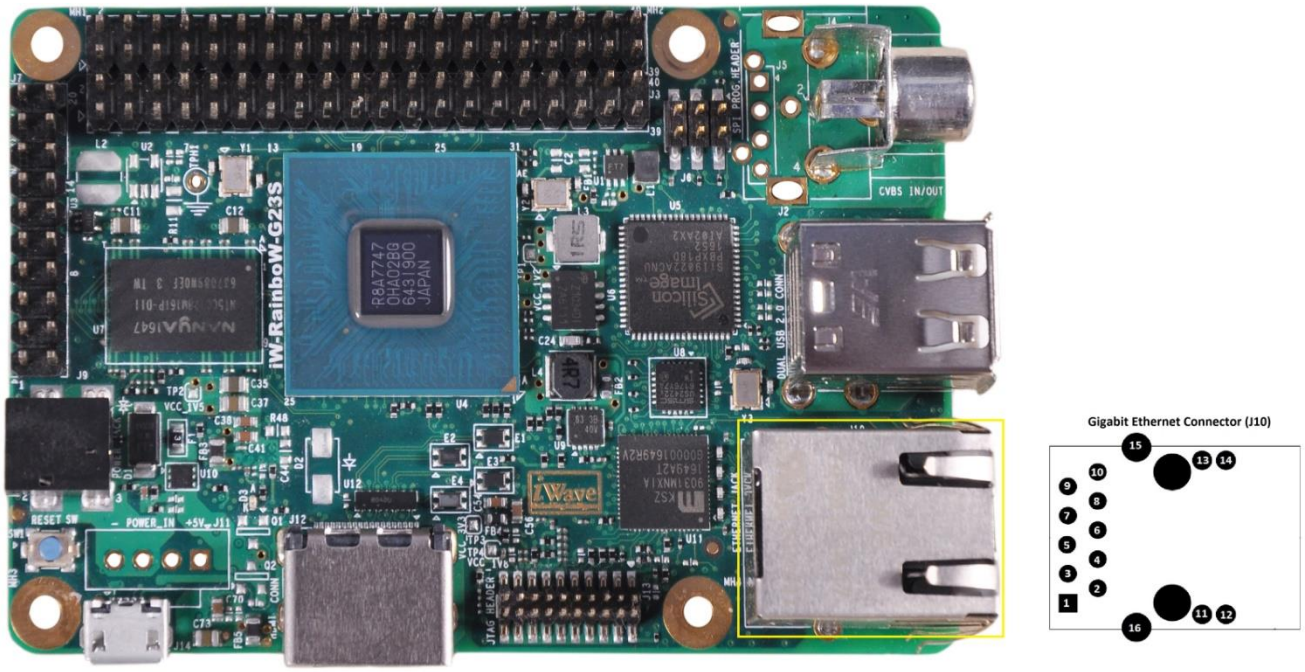


Figure 4: Gigabit Ethernet Connector

2.5.2 Dual USB 2.0 Host Ports

The RZ/G1C SBC supports two USB2.0 High Speed Host interface through RZ/G1C CPU's USB1 controller. This USB1 controller with integrated PHY supports USB2.0 High-Speed (480 Mbps)/Full-Speed (12 Mbps)/Low-Speed (1.5 Mbps) transfer. To support two USB2.0 Host interfaces, RZ/G1C CPU's USB1 controller is interfaced with two-port USB hub "USB2422". This Hub output port1 & port2 is connected to USB Type A Dual stack connector (J8). This Dual Stack Connector (J8) is physically located on top side of the SBC as shown below.

The VBUS power to the USB2.0 Host ports are connected through current limit power switch which limits the current above 500mA. Also over current output & power enable input of the current limit power switch is connected to corresponding USB HUB port's control pins to control the USB ports VBUS power.

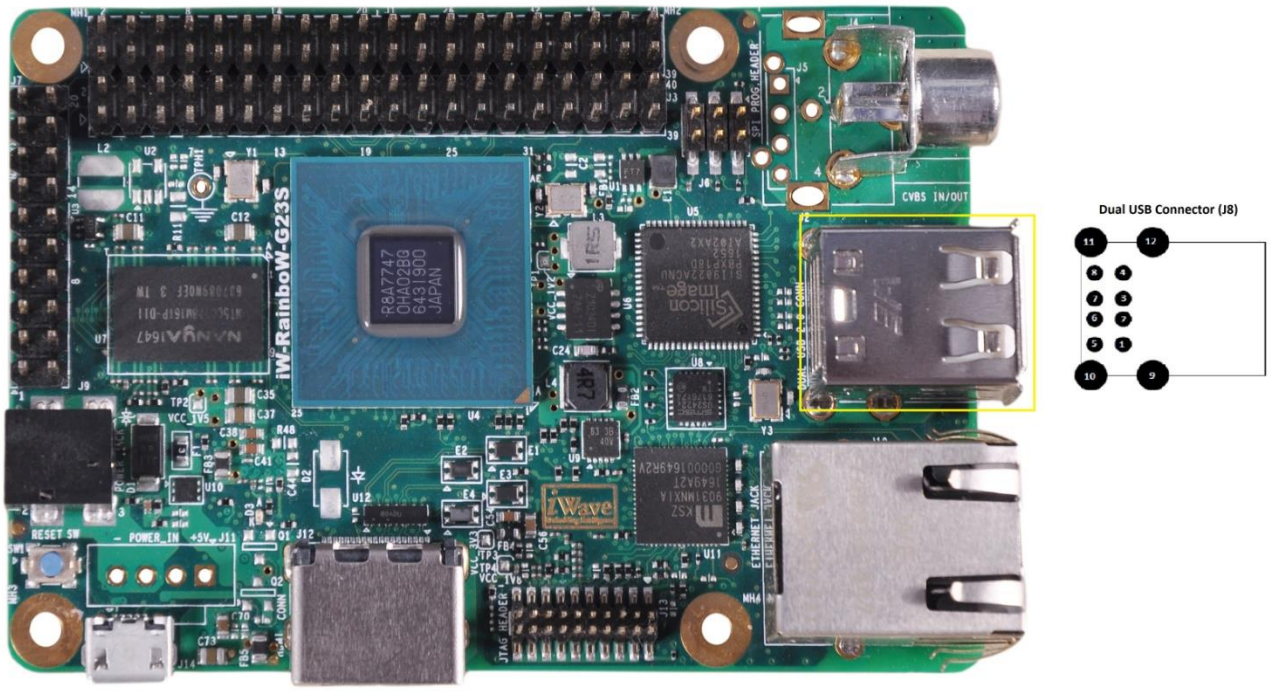


Figure 5: Dual USB 2.0 Host Connector

2.5.3 USB 2.0 Device Port

The RZ/G1C SBC supports one USB2.0 Device interface through RZ/G1C CPU's USB0 controller. This USB0 controller with integrated PHY which supports USB2.0 High-Speed (480 Mbps)/Full-Speed (12 Mbps)/Low-Speed (1.5 Mbps) transfer is directly connected to USB Micro B Connector (J14) and used in Function (Peripheral) mode. USB ID Pin from Micro B Connector is connected to RZ/G1C CPU's GPIO "GP0_1" pin. The Micro B Connector (J14) is physically located on top side of the SBC as shown below.

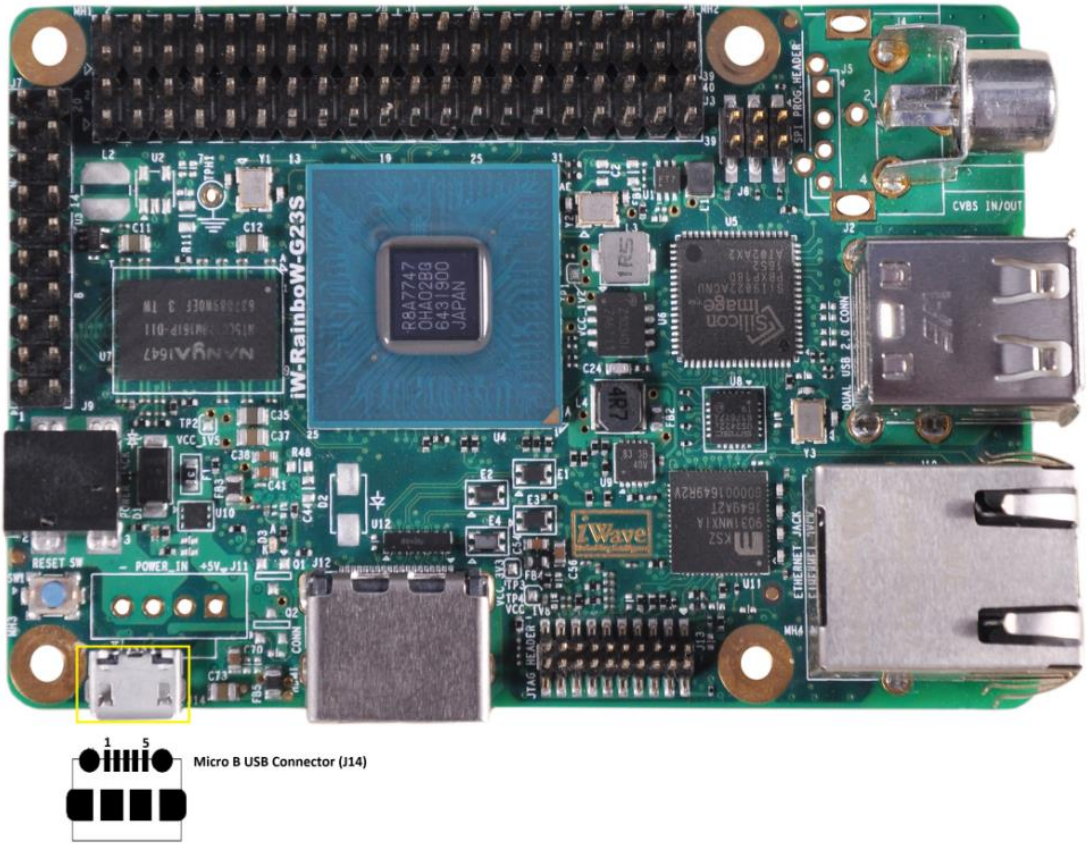


Figure 6: USB 2.0 Device Connector

2.6 Video Features

2.6.1 HDMI Port

The RZ/G1C CPU's display unit (DU) has two independently controllable channels DU0 & DU1 and supports RGB888 interface (24bpp), LVDS interface, and CVBS output interface. Using the DU0 and DU1, different images or the same image can be displayed on any two displays.

The RZ/G1C SBC supports one RGB888 interface for HDMI, one LVDS interface on Expansion Conenctor2 and optionally one CVBS output interface on RCA Jack. Upon these three interfaces, either two interfaces can be used at a time.

The RZ/G1C SBC supports HDMI output through on board RGB to HDMI Transmitter "SiI9022A". The RGB888 interface of RZ/G1C CPU DU0 controller is directly connected to HDMI Transmitter which supports video resolutions upto 1080p. Also RZ/G1C CPU's I2C4 interface is connected to HDMI Transmitter for control & configuration. The HDMI transmitter output is connected to Standard HDMI connector with ESD protection circuitry. HDMI Output connector (J12) is physically located on top of the SBC as shown below.

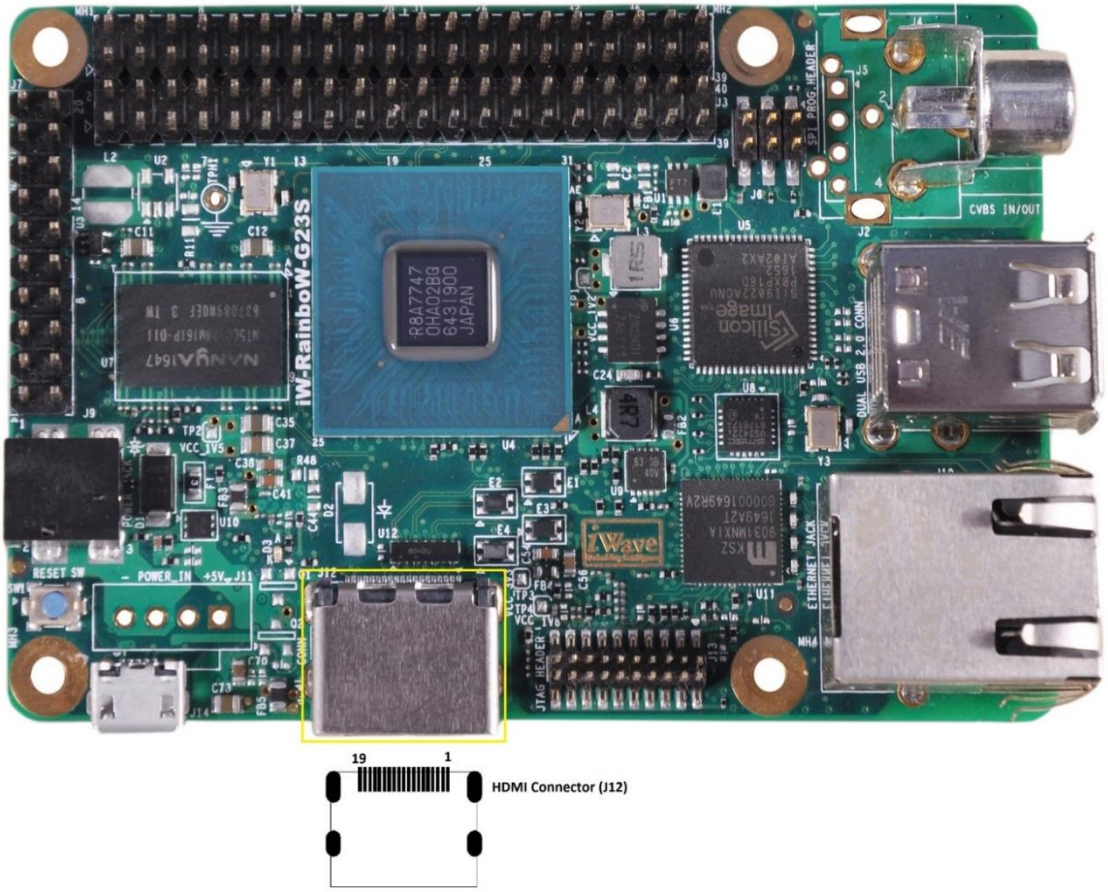


Figure 7: HDMI Connector

2.6.2 CVBS Input Port

The RZ/G1C SBC supports CVBS Input Interface through RZ/G1C CPU's digital video decoder module. This digital video decoder module consists of A/D convertor which converts CVBS input signal to digital format and connects to VIN module of the CPU. It supports NTSC, PAL & SECAM video input.

The RZ/G1C SBC has RCA Jack (J4) to support CVBS input signal and directly connects to the RZ/G1C CPU's VIN1A input. This CVBS IN RCA Jack (J4) is physically located at the top of the SBC as shown below.

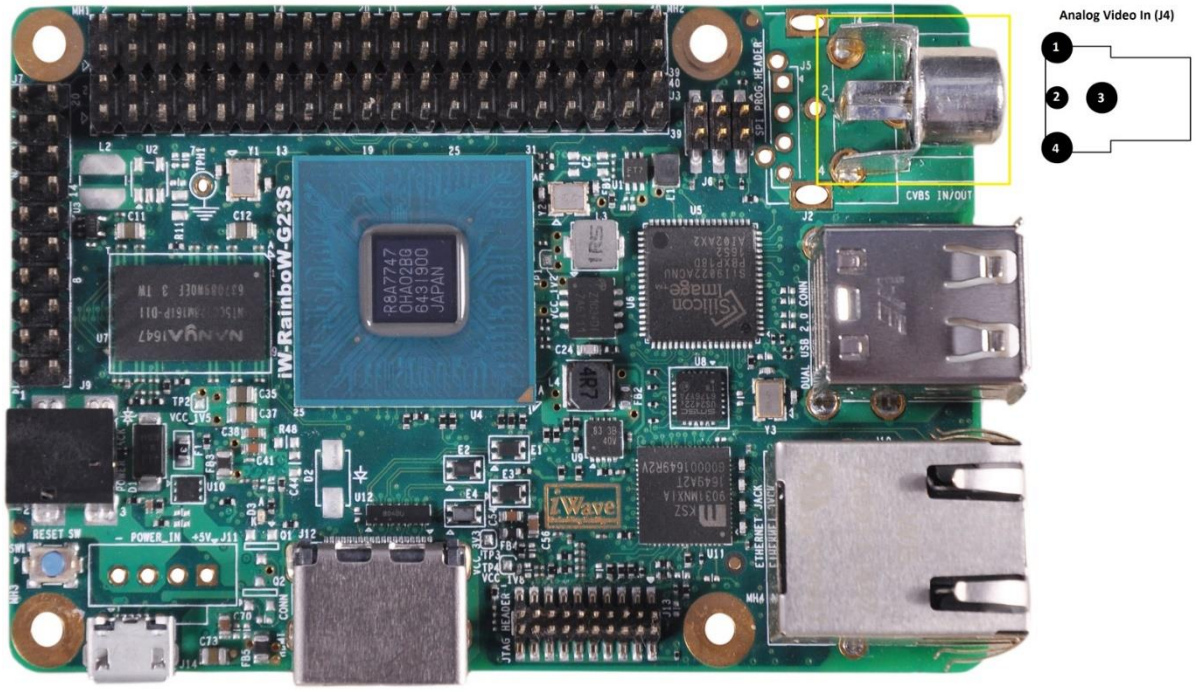


Figure 8: CVBS IN RCA Jack

2.6.3 CVBS Output Port (Optional)

The RZ/G1C SBC optionally supports CVBS Output Interface through RZ/G1C CPU's digital video encoder module. This digital video encoder module which connects from DU module incorporates the interlace DENC and outputs the encoded data to the Video DAC. It supports NTSC, PAL, PAL-M, PAL-N, and PAL-60 encode processing. The output of the Video DAC is directly connected to RCA JACK and by default not populated.

2.7 Other Features

2.7.1 JTAG Header

The RZ/G1C SBC supports JTAG Interface for CPU Debug purpose. A customized 20-pin ARM JTAG connector (J13) is available in SBC for JTAG interface. Even though this JTAG connector pinout is fully compatible with “ARM JTAG 20” connector, the physical dimension of connector is made smaller in RZ/G1C SBC because of space constraint.

RZ/G1C CPU’s JTAG pins are 1.8V tolerant and so 1.8V reference power is provided to pin 1 of the connector to allow JTAG tool to automatically configure the logic signals for the right voltage. The JTAG Connector (J13) is physically located at the top of the SBC as shown below.

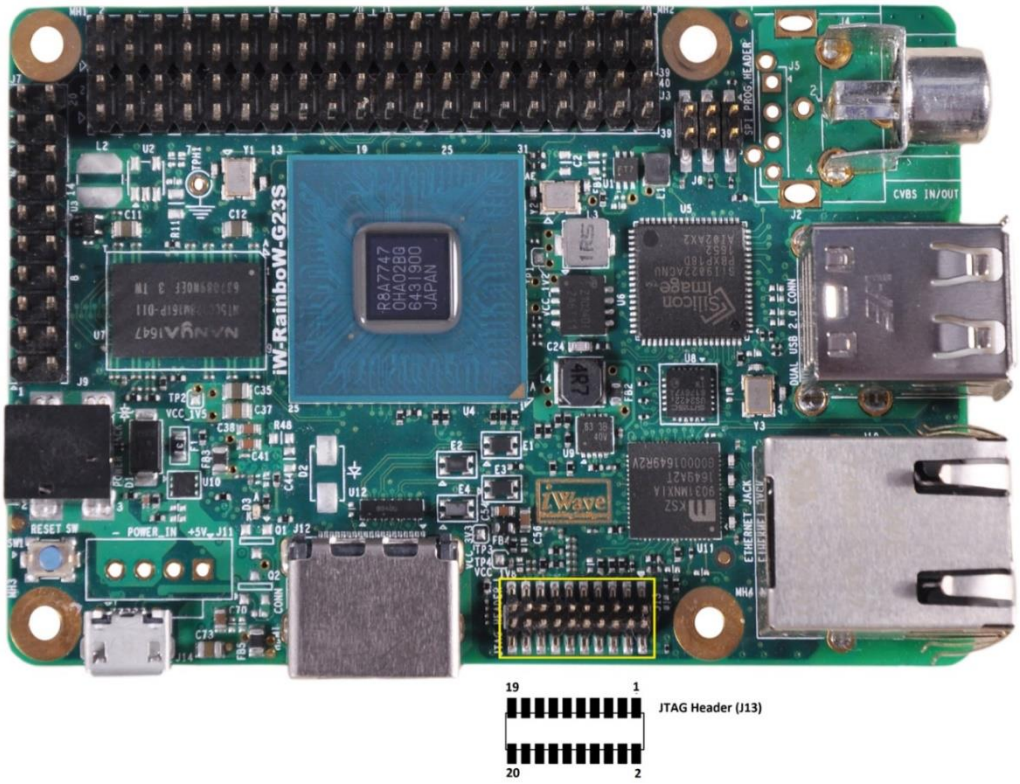


Figure 9: JTAG Connector

Table 3: JTAG Connector Pin Assignment

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VCC	VCC_1V8	O, 1.8V Power	VREF reference Voltage.
2	VCC	VCC_1V8	O, 1.8V Power	Supply Voltage.
3	JTAG_TRSTB	JTAG_TRSTB	I, 1.8V CMOS/ 10K PD	JTAG test reset signal.
4	GND	GND	Power	Ground.
5	JTAG_TDI	JTAG_TDI	I, 1.8V CMOS/ 4.7K PU	JTAG test data Input.
6	GND	GND	Power	Ground.
7	JTAG_TMS	JTAG_TMS	I, 1.8V CMOS/ 4.7K PU	JTAG test mode select.
8	GND	GND	Power	Ground.
9	JTAG_TCK	JTAG_TCK	I, 1.8V CMOS/ 4.7K PU	JTAG test clock.
10	GND	GND	Power	Ground.
11	NC	-	-	NC
12	GND	GND	Power	Ground.
13	JTAG_TDO	JTAG_TDO	O, 1.8V CMOS	JTAG test data Output.
14	GND	GND	Power	Ground.
15	JTAG_RESETB	JTAG_RESETB	I, 1.8V CMOS/ 1K PU	JTAG reset Signal.
16	GND	GND	Power	Ground.
17	NC	-	-	NC
18	GND	GND	Power	Ground.
19	NC	-	I, 1.8V CMOS/ 10K PD	Only pull down is provided.
20	GND	GND	Power	Ground.

2.7.2 SPI Flash Programming Header

To program the boot code in to the SPI flash for the first time, use JTAG debugger through JTAG Header (J13). Optionally the external SPI programmer through 6pin SPI Programming Header (J6) (or) with 8pin SOIC test clips (Example part: 923655-08 from 3M) can be used for programming the SPI flash.

The 6pin SPI Flash Programming Header is physically located on top side of the SBC as shown below.

Number of Pins - 6

Connector Part Number - 87759-0614

Mating Connector - 79107-7002 from Molex

Staking Height - 3.8mm

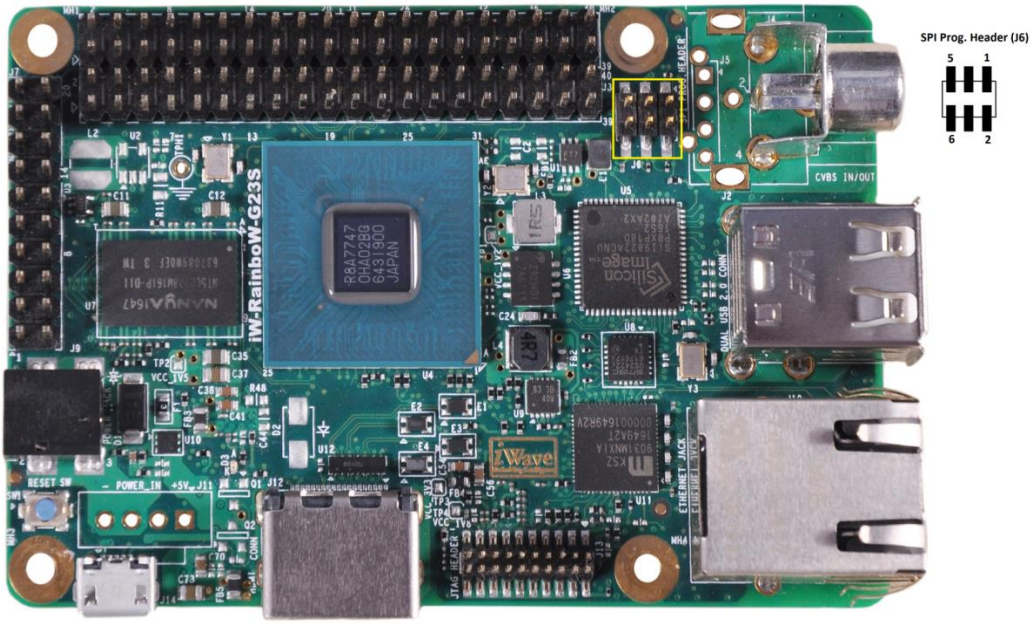


Figure 10: SPI Flash Programming Header

Table 4: SPI Flash Programming Header Pin Assignment

Pin No.	Signal Name	Signal Type/ Termination	Description
1	SPI_CS	I, 3.3V CMOS/ 10K PU	SPI Flash Chip Select.
2	SPI_SO	O, 3.3V CMOS	SPI Flash Serial Data Output.
3	GND	Power	Ground
4	SPI_SI	I, 3.3V CMOS	SPI Flash Serial Data Input.
5	SPI_SCK	I, 3.3V CMOS	SPI Flash Serial clock.
6	VCC_3V3	O, 3.3V Power	3.3V Power Supply.

2.7.3 Reset Switch

The RZ/G1C SBC supports Push button switch (SW1) to reset the RZ/G1C CPU. This Reset Push button switch (SW1) is physically located at the top of the SBC as shown below.

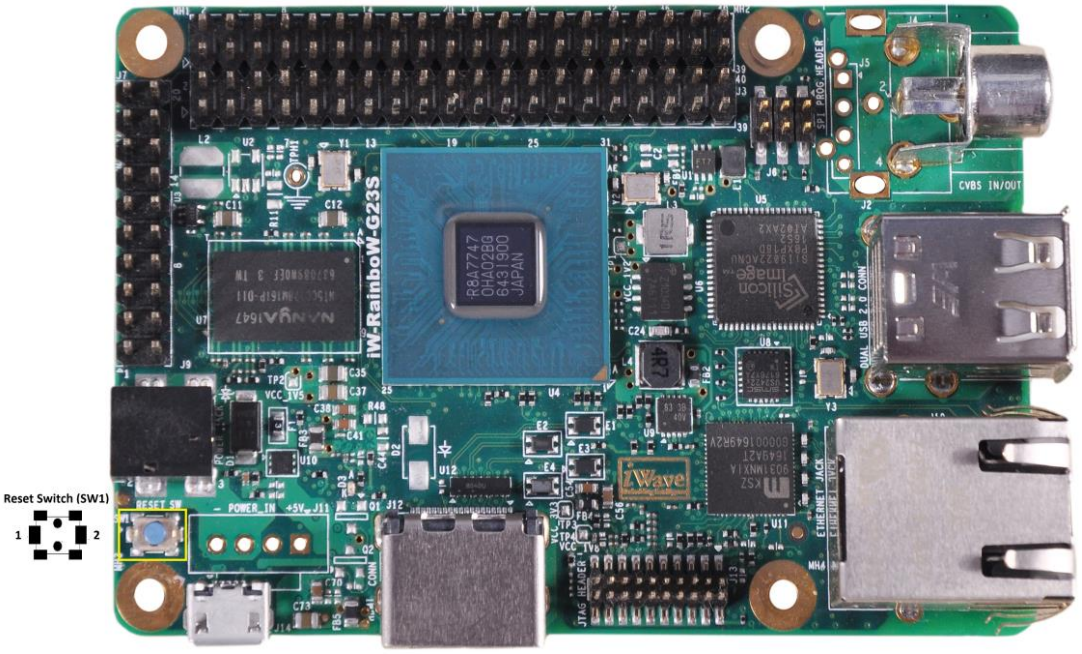


Figure 11: Reset Switch

2.8 Expansion Connector1 (40 Pin) Interfaces

The RZ/G1C SBC supports three Expansion connectors to pull out interfaces of RZ/G1C CPU. These three Expansion connectors includes two 40 pin Expansion connectors and one 20 pin Expansion Connector.

The interfaces which are available at 40 Pin Expansion connector1 are explained in the following sections. This Expansion Connector1 (J1) is physically located at the top of the SBC as shown below.

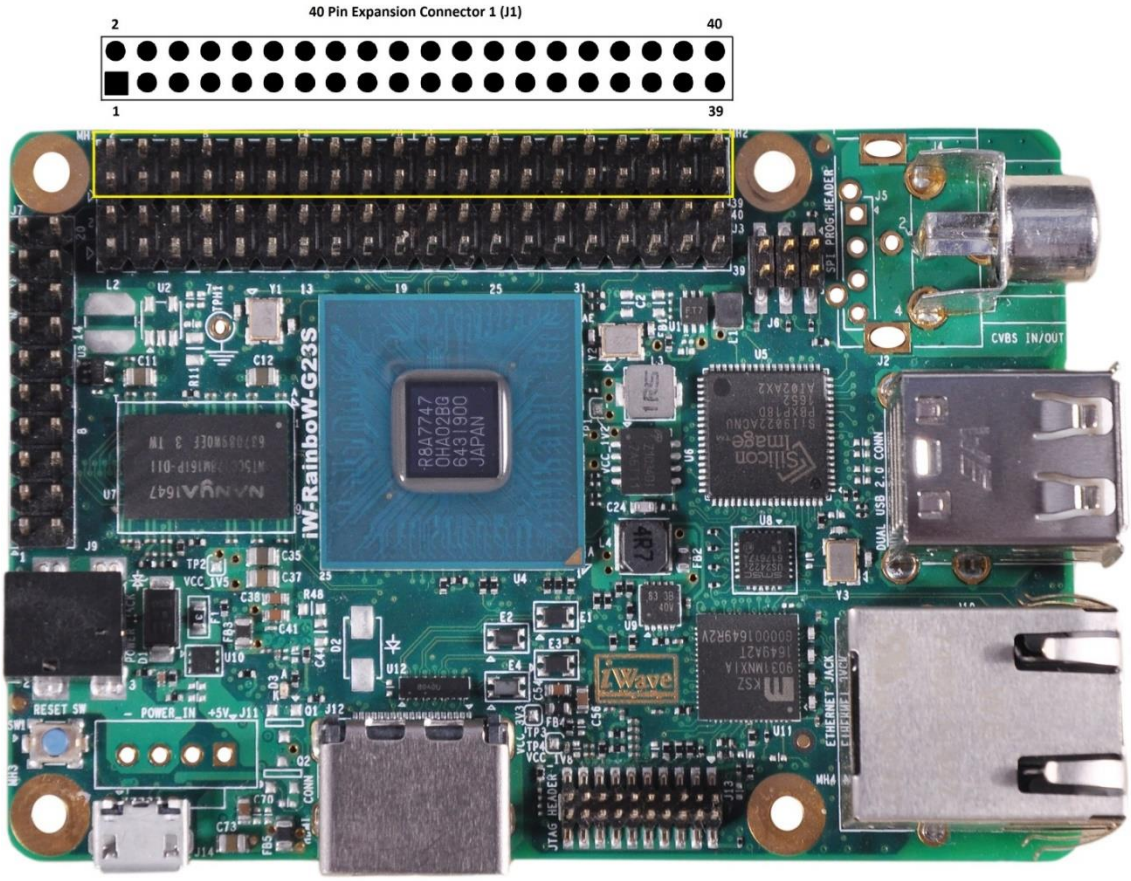


Figure 12: Expansion Connector1

Note: This connector pinout is compatible with Raspberry Pi connector pinout.

Number of Pins - 40

Connector Part Number - 61304021121

Mating Connector - 61304021821 from Wurth Electronics

Staking Height - 6mm

2.8.1 Data UART Interface

The RZ/G1C SBC supports one Data UART interface on Expansion connector1. RZ/G1C CPU's SCIF2 controller is used for Data UART interface with Transmit & Receive signal on Expansion connector1.

The RZ/G1C CPU's SCIF module has two 16-stage FIFO buffers separately for transmission and reception, which enables fast, efficient, and uninterrupted full duplex communication. It has On-chip baud rate generator that allows any bit rate to be selected. Also it supports DMA transfers.

For more details, refer Expansion connector1 pins 8 & 10 for SCIF2 on ***Table 5.***

2.8.2 SPI Interface

The RZ/G1C SBC supports one SPI interface on Expansion connector1. RZ/G1C CPU's MSIOF2 with two chip select is used for SPI interface which supports full-duplex synchronous four-wire serial interface with DMA.

The RZ/G1C CPU's MSIOF2 controller supports serial formats IIS, SPI (master and slave modes) at max speed of 26Mbps. It supports 32bit x 64 stages for transmit FIFOs & 32bit × 256 stages for receive FIFOs and allows MSB first or LSB first selectable for data transmission and reception.

For more details, refer Expansion connector1 pins 19, 21, 23, 24 & 26 pins for MSIOF2 on ***Table 5.***

2.8.3 I2C Interface

The RZ/G1C SBC supports two I2C interface on Expansion connector1. RZ/G1C CPU's I2C1 & I2C4 channels are used for I2C interface which is compatible with the standard NXP I2C bus protocol. It supports standard mode with data transfer rates up to 100kbps and Fast mode with data transfer rates up to 400kbps. It also supports Master/slave functions and Multi-master functions. RZ/G1C CPU I2C is not compliant with the 5V-input.

For more details, refer Expansion Connector1 pins 27 & 28 for I2C1 and 3 & 5 for I2C4 on ***Table 5.***

Note: I2C4 interface signals are also connected to On-board HDMI Transmitter with I2C address 0x72.

2.8.4 GPIO Interface

The RZ/G1C SBC supports many GPIOs (upto 17nos) on Expansion connector1.The RZ/G1C CPU's GPIO blocks provide general-purpose pins that can be configured as either input or output. When configured as an output, it is possible to write to an internal register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an internal register. In addition, the GPIO input can produce interrupt to the CPU core via the interrupt control block when corresponding registers are set.

For more details, refer Expansion Connector1 Pins 7, 11, 12, 13, 15, 16, 18, 22, 29, 31, 32, 33, 35, 36, 37, 38 & 40 for GPIOs on ***Table 5.***

Table 5: Expansion Connector1 Pin Assignment

Pin No.	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VCC_3V3	NA	O, 3.3V Power	3.3V Power Supply.
2	VCC_5V	NA	O, 5V Power	5V Power Supply.
3	I2C4_SDA(GP5_6)	SSI_SCK78_A/ D3	IO, 3.3V OD/ 1K PU	I2C4 Data. *Note: I2C4_SDA is connected to this Pin through resistor and default populated.* *Note: Same I2C4 is also connected to On-board HDMI transmitter.*
4	VCC_5V	NA	O, 5V Power	5V Power Supply.
5	I2C4_SCL(GP5_7)	SSI_WS78_A/ D2	O, 3.3V OD/ 1K PU	I2C4 Clock. *Note: I2C4_SCL is connected to this Pin through resistor and default populated.* *Note: Same I2C4 is also connected to On-board HDMI transmitter.*
6	GND	NA	Power	Ground.
7	GPIO(GP0_4)	CLKOUT/ AE2	IO, 3.3V CMOS	General purpose input/output.
8	SCIF2_TX2_B(GP5_26)	SSI_WS9_A/ K2	O,3.3V CMOS	SCIF2 Serial Communication Interface Serial Data Transmitter.
9	GND	NA	Power	Ground.
10	SCIF2_RX2_B(GP5_25)	SSI_SCK9_A/ K3	I, 3.3V CMOS	SCIF2 Serial Communication Interface Serial Data Receiver.
11	GPIO(GP4_8)	MSIOF0_SS1_A/ C6	IO, 3.3V CMOS	General purpose input/output.
12	GPIO(GP4_9)	MSIOF0_SS2_A/ D6	IO, 3.3V CMOS	General purpose input/output.
13	GPIO(GP5_15)	SSI_SCK4_A/ G4	IO, 3.3V CMOS	General purpose input/output.
14	GND	NA	Power	Ground.
15	GPIO(GP5_21)	SSI_SDATA1_A/ J4	IO, 3.3V CMOS	General purpose input/output.
16	GPIO(GP2_26)	DU0_DOTCLKOUT1/AB11	IO, 3.3V CMOS	General purpose input/output.
17	VCC_3V3	NA	O, 3.3V Power	3.3V Power Supply.
18	GPIO(GP1_22)	EX_WAIT0/ AE3	IO, 3.3V CMOS	General purpose input/output.
19	MSIOF2_TXD_A(GP1_11)	D11/ Y5	O,3.3V CMOS	SPI Master serial output/Slave serial output (MSIOF2).
20	GND	NA	Power	Ground.
21	MSIOF2_RXD_A(GP1_10)	D10/ AA1	I,3.3V CMOS	SPI Master serial input /Slave serial output (MSIOF2).

Pin No.	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
22	GPIO(GP5_24)	SSI_SDATA2_A/ J1	IO, 3.3V CMOS	General purpose input/output.
23	MSIOF2_SCK_A(GP1_12)	D12/ Y4	O, 3.3V CMOS	SPI Serial clock (MSIOF2).
24	MSIOF2_SYNC	D13/ Y3	O, 3.3V CMOS	SPI frame synchronization signal/ SPI chip select0 (MSIOF2).
25	GND	NA	Power	Ground.
26	MSIOF2_SS1(GP1_14)	D14/ Y2	IO,3.3V CMOS	SPI frame synchronization signal/ SPI chip select1 (MSIOF2).
27	I2C1_SDA1_C(GP4_23)	TX3_A/ A4	IO, 3.3V OD/ 1K PU	I2C1 Data.
28	I2C1_SCL1_C(GP4_22)	RX3_A/ B3	O, 3.3V OD/ 1K PU	I2C1 Clock.
29	GPIO(GP1_4)	D4/ AB3	O,3.3V CMOS	General purpose input/output. *Note: The same signal can also be used as PWM6.*
30	GND	NA	Power	Ground.
31	GPIO(GP4_7)	MSIOF0_SYNC_ A/B5	IO, 3.3V CMOS	General purpose input/output.
32	GPIO(GP1_15)	D15/ Y1	IO,3.3V CMOS	General purpose input/output. *Note: The same signal can also be used as SPI chip selecet2 for MSIOF2*
33	GPIO(GP5_29)	AUDIO_CLKB_A/ E3	IO, 3.3V CMOS	General purpose input/output.
34	GND	NA	Power	Ground.
35	GPIO(GP4_25)	SDA2_A/ C4	IO, 3.3V CMOS	General purpose input/output.
36	GPIO(GP0_0)	USB0_PWEN/ Y22	IO, 3.3V CMOS	General purpose input/output.
37	GPIO(GP4_24)	SCL2_A/ B4	IO, 3.3V CMOS	General purpose input/output.
38	GPIO(GP1_20)	QSPI0_IO3/ AC5	IO, 3.3V CMOS	General purpose input/output. *Note: GP1_20 is connected to this pin through resistor and default populated.* *Note: Optionally GP0_2 is connected to this pin thorough resistor and default not populated.*
39	GND	NA	Power	Ground.
40	GPIO(GP5_0)	SSI_SCK5_A/ A3	IO, 3.3V CMOS	General purpose input/output.

2.9 Expansion Connector2 (40 Pin) Interfaces

The interfaces which are available at 40 Pin Expansion connector2 are explained in the following sections. This Expansion Connector2 (J3) is physically located at the top of the SBC as shown below.

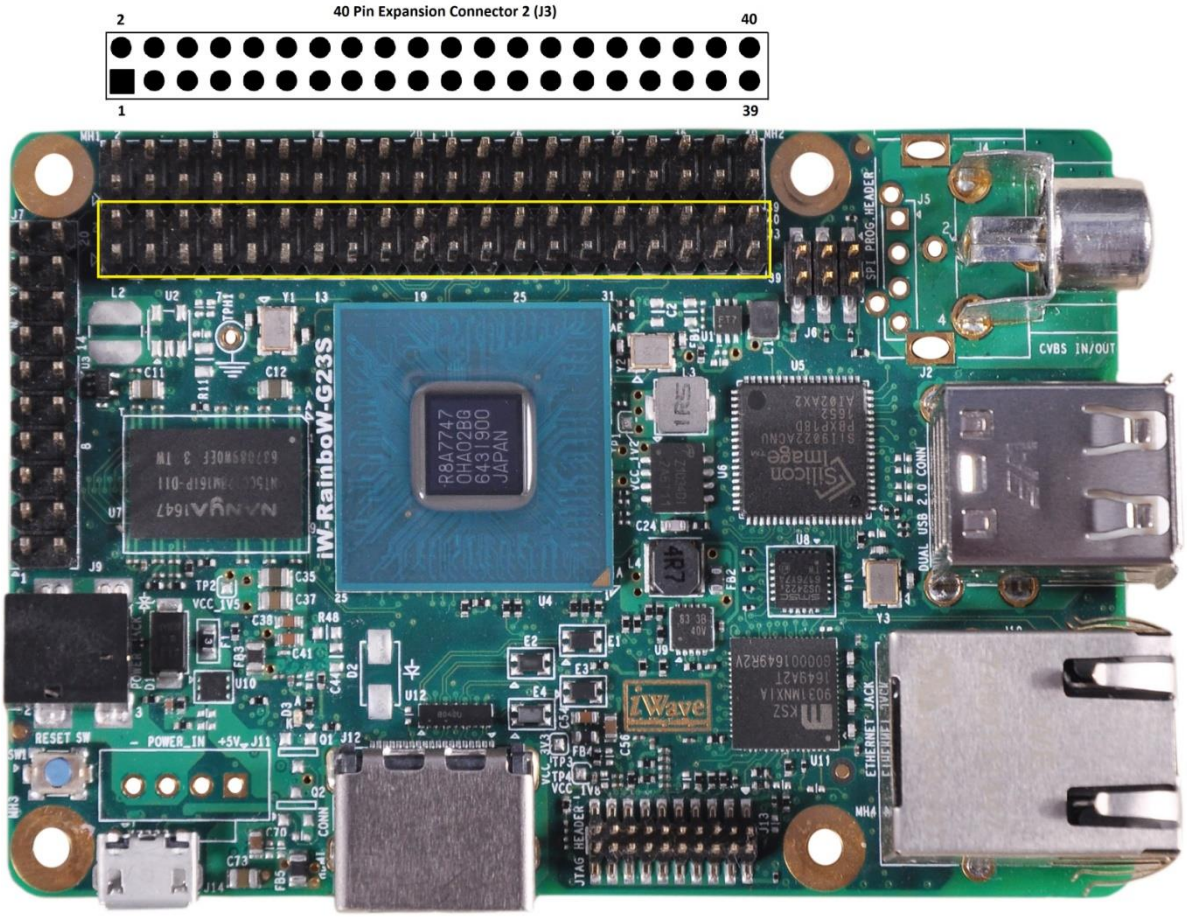


Figure 13: Expansion Connector2

Number of Pins - 40

Connector Part Number - 61304021121

Mating Connector - 61304021821 from Wurth Electronics

Staking Height - 6mm

2.9.1 LVDS Interface

The RZ/G1C SBC supports one LVDS interface on Expansion Conenctor2. The RZ/G1C CPU's LVDS module is used for LVDS interface which supports five differential output pairs (4 data and 1 clock) that conform to the TIA/EIA-644 standard with dot clock operating frequency of 13.40 to 87 MHz. The LVDS interface supports 8 output data formats which can be selected by register settings.

For more details, refer Expansion connector2 pins 7, 9, 13, 15, 19, 21, 25, 27, 31 & 33 for LVDS interface on ***Table 6.***

Note: The RZ/G1C SBC optionally supports on board LED driver "LM3410XMF" to drive the backlight of LVDS LCDs. This LED driver output is optionally connected to 2nd pin & 4th pin of Expansion Conenctor2 through resistor and default not populated.

2.9.2 CAN Interface

The RZ/G1C SBC supports one CAN interface on Expansion connector2. RZ/G1C CPU's CAN module supports two channels in which CAN0 channel is connected to Expansion connector2.

The RZ/G1C CPU's CAN module complies with the ISO11898-1 Specifications and supports programmable bit rate up to 1 Mbps with both formats of messages namely the standard identifier (11 bits) and extended ID (29 bits). It also supports 64 mailboxes in two selectable mailbox mode Normal mailbox mode and FIFO mailbox mode. To connect external CAN module to this bus, it is necessary to add transceiver in between.

For more details, refer Expansion connector2 pins 14 & 16 for CAN0 on ***Table 6.***

2.9.3 I2S Audio Interface

The RZ/G1C Supports two I2S audio interface port on Expansion connector2. RZ/G1C CPU's SSI1 and SSI0/9 of SSIU are used for I2S interface.

The RZ/G1C CPU's serial sound interface (SSI) is a transceiver module designed to send or receive audio data interfacing with a variety of devices offering I2S format. It also supports master/slave functions and multi-channel format functions. The frequency range of SCK signal is from 297.3 kHz to 12.5 MHz at master mode and from 297.3kHz to 15.1 MHz at slave mode. SSI Module supports TDM format operation at 44.1 or 48kHz sampling rate.

For more details, refer Expansion connector2 pins 1, 3 & 5 for SSI1 and 6, 8, 10 & 12 for SSI0/9 on ***Table 6.***

2.9.4 Data UART Interface

The RZ/G1C SBC supports three Data UART interface on Expansion connector2. RZ/G1C CPU's SCIF5 controller is used for Data UART interface with Transmit & Receive signal on Expansion connector2. RZ/G1C CPU's HSCIF1 and HSCIF2 controller is used for Data UART interface with hardware flow control for request to send and clear to send signals on Expansion connector2.

The RZ/G1C CPU's SCIF module has two 16-stage FIFO buffers separately for transmission and reception, which enables fast, efficient, and uninterrupted full duplex communication. It has On-chip baud rate generator that allows any bit rate to be selected. Also it supports DMA transfers.

The RZ/G1C CPU's HSCIF1 and HSCIF2 is a high speed serial communication interface with built-in FIFO buffers that handles asynchronous communication. It has two 128-stage FIFO buffers separately for transmission and reception, which enables fast, efficient, and uninterrupted communication.

For more details, refer Expansion connector2 pins 28 & 30 for SCIF5, 32, 34, 36 & 38 for HSCIF1 and 18, 20, 22, 24 & 26 for HSCIF2 on ***Table 6.***

2.9.5 I2C Interface

The RZ/G1C SBC supports one I2C interface on Expansion connector2. RZ/G1C CPU's I2C3 channel is used for I2C interface which is compatible with the standard NXP I2C bus protocol. It supports standard mode with data transfer rates up to 100kbps and Fast mode with data transfer rates up to 400kbps. It also supports Master/slave functions and Multi-master functions. RZ/G1C CPU is not compliant with the 5V-input.

For more details, refer Expansion connector2 pins 37 & 39 for I2C3 on ***Table 6.***

2.9.6 PWM Interface

The RZ/G1C SBC supports one PWM interface on Expansion Connector2. RZ/G1C CPU's PWM0 channel is used for PWM interface. This PWM timer has a 10-bit counter and supports configurable PWM output cycle within the range from 2 cycles to 2^{24} × 1024 cycles of internal bus clock (i.e. from 30.77 ns to 264 seconds when bus clock = 65 MHz). Also it supports continuous pulse output mode or single pulse output mode which is configurable.

For more details, refer Expansion connector2 pin 40 for PWM0 on ***Table 6.***

Table 6: Expansion Connector2 Pin Assignment

Pin No.	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	SSI_SCK1_C(GP0_5)	SD0_CLK/ A13	O, 3.3V CMOS	Audio Serial clock for SSI channel 1.
2	VCC_3V3	NA	O, 3.3V Power	3.3V Power Supply. *Note: 3.3V power is connected to this pin through resistor and default populated.* *Note: Optionally LED driver Output negative is connected to this pin through resistor and default not populated.*
3	SSI_SDATA1_C(GP0_7)	SD0_DAT0/B13	IO, 3.3V CMOS	Audio Serial data for SSI channel 1.
4	VCC_5V	NA	O, 5V Power	5V Power Supply. *Note: 5V power is connected to this pin through resistor and default populated.* *Note: Optionally LED driver Output positive is connected to this pin through resistor and default not populated.*
5	SSI_WS1_C(GP0_6)	SD0_CMD/ D13	IO, 3.3V CMOS	Audio Word select for SSI channel 1.
6	SSI_SCK0129_B(GP0_8)	SD0_DAT1/ D14	IO, 3.3V CMOS	Audio Serial clock for SSI channel 0/1/2/9.
7	TXOUT3P	TXOUT3P/ AD17	O, 3.3V LVDS	LVDS data output3 positive.
8	SSI_SDATA0_B(GP0_10)	SD0_DAT3/ B14	IO, 3.3V CMOS	Audio Serial data for SSI channel 0.
9	TXOUT3M	TXOUT3M/ AE17	O, 3.3V LVDS	LVDS data output3 negative.
10	SSI_WS0129_B(GP0_9)	SD0_DAT2/ C14	IO, 3.3V CMOS	Audio Word select for SSI channel 0.
11	GND	NA	Power	Ground.
12	SSI_SDATA9_B(GP4_21)	SD2_WP/ D8	IO, 3.3V CMOS	Audio Serial data for SSI channel 9.
13	TXCLKOUTP	TXCLKOUTP/ AB16	O, 3.3V LVDS	LVDS clock output positive.
14	CAN0_RX_A(GP0_11)	SD0_CD/ A8	I, 3.3V CMOS	Receive input for CAN channel0.
15	TXCLKOUTM	TXCLKOUTM/ AC16	O, 3.3V LVDS	LVDS clock output negative.
16	CAN0_TX_A(GP0_12)	SD0_WP/ B8	O, 3.3V CMOS	Transmit output for CAN channel0.
17	GND	NA	Power	Ground.
18	HSCIF2_HCTS2(GP1_8)	D8/ AA3	I, 3.3V CMOS	High Speed Serial Communication Interface (HSCIF2) Clear to Send.

Pin No.	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
19	TXOUT2P	TXOUT2P/ AD15	O, 3.3V LVDS	LVDS data output2 positive.
20	HSCIF2_HRTS2(GP1_9)	D9/ AA2	O, 3.3V CMOS	High Speed Serial Communication Interface (HSCIF2) Ready to Send.
21	TXOUT2M	TXOUT2M/ AE15	O, 3.3V LVDS	LVDS data output2 negative.
22	HSCIF2_HRX2(GP1_5)	D5/ AB2	I, 3.3V CMOS	High Speed Serial Communication Interface (HSCIF2) Serial Data Receiver.
23	GND	NA	Power	Ground.
24	HSCIF2_HTX2(GP1_6)	D6/ AB1	O, 3.3V CMOS	High Speed Serial Communication Interface (HSCIF2) Serial Data Transmitter.
25	TXOUT1P	TXOUT1P/ AB14	O, 3.3V LVDS	LVDS data output1 positive.
26	HSCIF2_HSCK2(GP1_7)	D7/ AA4	IO, 3.3V CMOS	High Speed Serial Communication Interface (HSCIF2) clock.
27	TXOUT1M	TXOUT1M/ AC14	O, 3.3V LVDS	LVDS data output1 negative.
28	SCIF5_RX5_B(GP1_0)	D0/ AD2	I, 3.3V CMOS	Serial Communication Interface (SCIF5) Serial Data Receiver.
29	GND	NA	Power	Ground.
30	SCIF5_TX5_B(GP1_1)	D1/ AD1	O, 3.3V CMOS	Serial Communication Interface (SCIF5) Serial Data Transmitter.
31	TXOUT0P	TXOUT0P/ AD13	O, 3.3V LVDS	LVDS data output0 positive.
32	HSCIF1_HCTS1_A(GP4_12)	HCTS1#_A/ E8	I, 3.3V CMOS	High Speed Serial Communication Interface (HSCIF1) Clear to Send.
33	TXOUT0M	TXOUT0M/ AE13	O, 3.3V LVDS	LVDS data output0 negative.
34	HSCIF1_HRTS1_A(GP4_13)	HRTS1#_A/ D7	O, 3.3V CMOS	High Speed Serial Communication Interface (HSCIF1) Ready to Send.
35	PRESETOUT#	PRESETOUT#/ AC20	O, 3.3V CMOS	Reset Output. *Note: PRESETOUT# is connected to this pin through resistor and default populated.* *Note: Optionally GP1_19 pin is connected to this pin through resistor and default not populated.*
36	HSCIF1_HTX1_A(GP4_11)	HTX1_A/ B7	O, 3.3V CMOS	High Speed Serial Communication Interface (HSCIF1) Serial Data Transmitter.

Pin No.	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
37	I2C3_SCL(GP5_1)	SSI_WS5_A/ A2	O, 3.3V OD/ 1K PU	I2C3 Clock.
38	HSCIF1_HRX1_A(GP4_10)	HRX1_A/ A7	I, 3.3V CMOS	High Speed Serial Communication Interface (HSCIF1) Serial Data Receiver.
39	I2C3_SDA(GP5_2)	SSI_SDATA5_A/ B2	IO, 3.3V OD/ 1K PU	I2C3 Data.
40	PWM0_C(GP5_11)	SSI_SDATA0_A/ H4	O,3.3V CMOS	Pulse Width Modulated output 0.

2.10 Expansion Connector3 (20 Pin) Interfaces

The interfaces which are available at 20 Pin Expansion connector3 are explained in the following sections. This Expansion Connector3 (J7) is physically located at the top of the SBC as shown below.

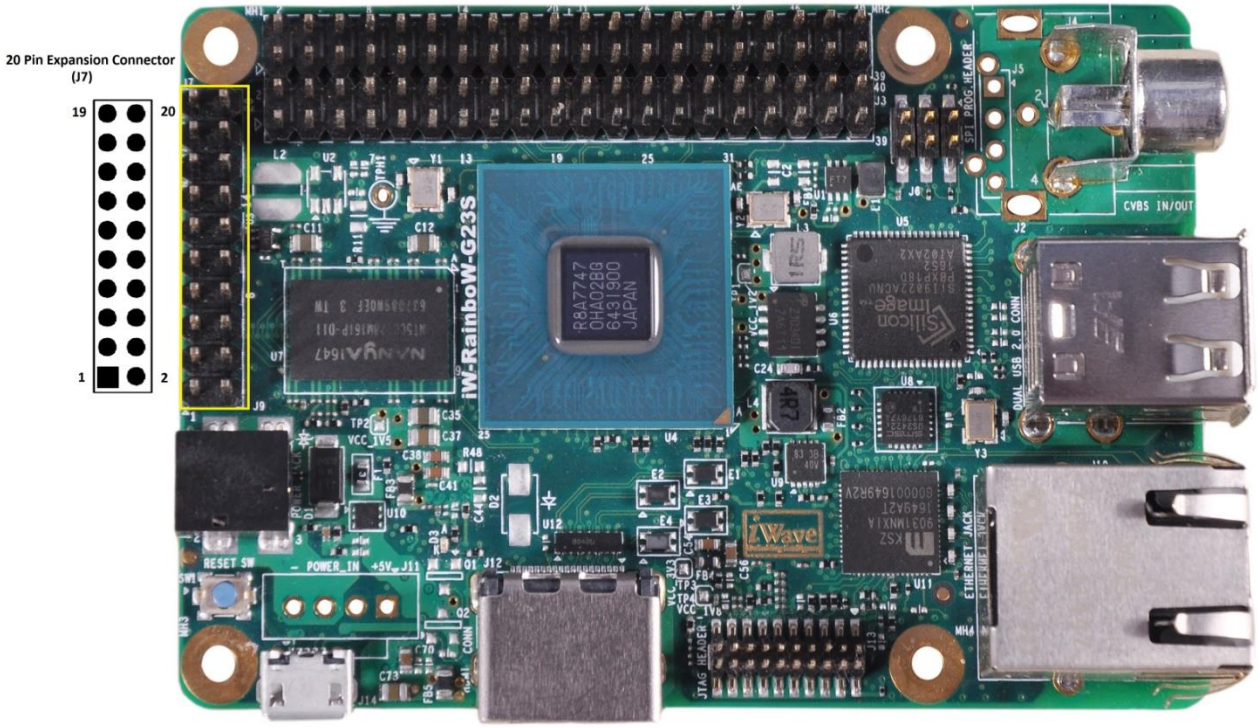


Figure 14: Expansion Connector3

Number of Pins - 20

Connector Part Number - 61302021121

Mating Connector - 61302021821 from Wurth Electronics

Staking Height - 6mm

2.10.1 Debug UART Interface

The RZ/G1C SBC supports Debug UART interfaces on Expansion connector3. RZ/G1C CPU's SCIF1 controller is used for Debug UART. If Debug UART interface is not required, then same SCIF1 can be used for Data UART interface.

The RZ/G1C CPU's SCIF module has two 16-stage FIFO buffers separately for transmission and reception, which enables fast, efficient, and uninterrupted full duplex communication. It has On-chip baud rate generator that allows any bit rate to be selected. Also it supports DMA transfers.

For more details, refer Expansion connector3 pins 17 & 19 for SCIF1 Debug UART interface on ***Table 7.***

2.10.2 Data UART/I2C Interface

The RZ/G1C SBC supports one Data UART interfaces on Expansion connector3. RZ/G1C CPU's SCIF4 controller is used for Data UART interface.

The RZ/G1C CPU's SCIF module has two 16-stage FIFO buffers separately for transmission and reception, which enables fast, efficient, and uninterrupted full duplex communication. It has On-chip baud rate generator that allows any bit rate to be selected. Also it supports DMA transfers.

For more details, refer Expansion connector3 pins 18 & 20 for SCIF4 on ***Table 7.***

Note: If Data UART interface is not required on these pins, then the same pins can be configured as I2C0 interface. Make sure to add the pullup resistors externally when these pins are used as I2C0.

2.10.3 Parallel Camera Interface

The RZ/G1C SBC supports one 8bit parallel camera interface. RZ/G1C CPU VIN0 channel is used for this 8bit parallel camera interface and directly connected to Expansion Connector3.

The RZ/G1C CPU's Video Input Module (VIN0) is a video capture module that supports YCbCr-422 data through the ITU-R BT.601, ITU-R BT.656 or ITU-R BT.709 interface and RGB data through the ITUR BT.601 or ITU-R BT.709 interface. The VIN0 supports Vertical and Horizontal Scaling where the image can be scaled up and down up to three times in the vertical and two times in the horizontal directions. Also, it has two clipping circuits, which independently handle images with up to 2048 × 2048 pixels. The VIN provides a colour space conversion function from YCbCr-422 to RGB, a format conversion function from RGB to ARGB.

For more details, refer Expansion connector3 pins 1,2,3,4,8,9,10,11,12,13,14 & 16 for VIN0 on ***Table 7***

2.10.4 PWM Interface

The RZ/G1C SBC supports one PWM interface on Expansion Connector3. RZ/G1C CPU's PWM2 channel is used for PWM interface. This PWM timer has a 10-bit counter and supports configurable PWM output cycle within the range from 2 cycles to 2^{24} × 1024 cycles of internal bus clock (i.e. from 30.77 ns to 264 seconds when bus clock = 65 MHz). Also it supports continuous pulse output mode or single pulse output mode which is configurable.

For more details, refer Expansion connector3 pin 7 for PWM2 on ***Table 7***

Table 7: Expansion Connector3 Pin Assignment

Pin No.	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VI0_CLK/AVB_COL(GP5_18)	SSI_SCK1_A/ H2	I, 3.3V CMOS	Video Input Channel0 pixel clock. *Note: This signal is optionally connected to Ethernet PHY Collision pin through resistor and default not populated.*
2	VI0_HSYNC(GP5_30)	AUDIO_CLKC_A/ E4	I, 3.3V CMOS	Video Input Channel0 Horizontal synchronization signal.
3	VI0_VSYNC(GP5_31)	AUDIO_CLKOUT_A/E1	I, 3.3V CMOS	Video Input Channel0 Vertical synchronization signal.
4	VI0_CLKENB(GP5_28)	AUDIO_CLKA_A/ E2	I, 3.3V CMOS	Video Input Channel0 data enable signal.
5	GND	GND	Power	Ground.
6	VCC	VCC_5V	O, 5V Power	5V Power Supply.
7	PWM2_D(GP5_27)	SSI_SDATA9_A/ K1	O, 3.3V CMOS	Pulse Width Modulated output 2. *Note: PWM2 signal is connected to this pin through resistor and default populated.* *Note: Optionally same signal is connected to LED driver DIM pin through resistor and default not populated.*
8	VI0_G2(GP4_4)	MSIOF0_RXD_A /A6	I, 3.3V CMOS	Video Input0 Data 2.
9	VI0_G4(GP4_6)	MSIOF0_SCK_A/ A5	I, 3.3V CMOS	Video Input0 Data 4.
10	VI0_G3(GP4_5)	MSIOF0_TXD_A/ B6	I, 3.3V CMOS	Video Input0 Data 3.
11	VI0_G7(GP5_10)	SSI_WS0129_A/ G1	I, 3.3V CMOS	Video Input0 Data 7.
12	VI0_G0(GP4_2)	SCL1_A/ C5	I, 3.3V CMOS	Video Input0 Data 0.
13	VI0_G1(GP4_3)	SDA1_A/ D5	I, 3.3V CMOS	Video Input0 Data 1.
14	VI0_G5(GP5_8)	SSI_SDATA7_A/ F5	I, 3.3V CMOS	Video Input0 Data 5.
15	GND	GND	Power	Ground.
16	VI0_G6(GP5_9)	SSI_SCK0129_A/ G2	I, 3.3V CMOS	Video Input0 Data 6.
17	SCIF1_RX1_B(GP5_19)	SSI_SDATA8_A/ F4	I, 3.3V CMOS	SCIF1 Serial data receiver input for debug.
18	SCIF4_RX4_B(GP1_2)	D2/ AC2	I, 3.3V CMOS	SCIF4 Serial data receiver input.

Pin No.	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
19	SCIF1_TX1_B(GP5_20)	SSI_WS1_A/ H1	O, 3.3V CMOS	SCIF1 Serial data transmitter output for debug.
20	SCIF4_TX4_B(GP1_3)	D3/ AC1	O, 3.3V CMOS	SCIF4 Serial data transmitter output.

2.11 RZ/G1C Pin Multiplexing on Expansion Connectors

The RZ/G1C CPU IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement. Also most of the RZ/G1C CPU's IO pins can be configured as GPIO if required. The below table provides the details of RZ/G1C CPU pin connections to the Expansion connectors with selected pin function highlighted and available alternate functions. This table has been prepared by referring Renesas's RZ/G1C Hardware User's Manual.

Table 8: RZ/G1C CPU IOMUX for Expansion Connector1 Interfaces

Interface/ Function	Expansion Connnector1 Pin Numbers	RZ/G1C CPU Pin Number	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	GPIO	Default State
SCIF2	8	K2	SSI_WS9_A	TX2_B	SDA3_E				VI0_DATA6_ VI0_B6		GP5_26	GP5_26
	10	K3	SSI_SCK9_A	RX2_B	SCL3_E			EX_WAIT1	VI0_DATA5_ VI0_B5		GP5_25	GP5_25
MSIOF2	19	Y5	D11	MSIOF2_TXD _A	HTX0_B						GP1_11	GP1_11
	21	AA1	D10	MSIOF2_RXD _A	HRX0_B						GP1_10	GP1_10
	23	Y4	D12	MSIOF2_SCK _A	HSCK0		CAN_CLK_C				GP1_12	GP1_12
	24	Y3	D13	MSIOF2_SYN C_A		RX4_C					GP1_13	GP1_13
	26	Y2	D14	MSIOF2_SS1		TX4_C	CAN1_RX_B		AVB_AVTP_C APTURE_A		GP1_14	GP1_14
I2C1	27	A4	TX3_A	SDA1_C	MSIOF1_TXD _B	DU1_DB5	AUDIO_CLKB _C	SSI_WS4_B			GP4_23	GP4_23
	28	B3	RX3_A	SCL1_C	MSIOF1_RXD _B	DU1_DB4	AUDIO_CLKA _C	SSI_SDATA4_ B			GP4_22	GP4_22
I2C4	3	D3	SSI_SCK78_A		SDA4_E	DU1_DISP					GP5_6	GP5_6
	5	D2	SSI_WS78_A		SCL4_E	DU1_CDE					GP5_7	GP5_7

Interface/ Function	Expansion Connnector1 Pin Numbers	RZ/G1C CPU Pin Number	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	GPIO	Default State
GPIOs	11	C6	MSIOF0_SS1_A		Reserved	DU1_DR6	Reserved	QSPI1_IO3	SSI_SDATA8_B		GP4_8	GP4_8
	13	G4	SSI_SCK4_A		AVB_MAGIC				VI0_R4		GP5_15	GP5_15
	15	J4	SSI_SDATA1_A	HRX1_B					VI0_DATA1_VI0_B1		GP5_21	GP5_21
	31	B5	MSIOF0_SYNC_A	PWM1_A	Reserved	DU1_DR5	Reserved	QSPI1_IO2	SSI_SDATA7_B		GP4_7	GP4_7
	33	E3	AUDIO_CLKB_A	SDA0_B	Reserved	TANS2			VI0_FIELD		GP5_29	GP5_29
	35	C4	SDA2_A		MSIOF1_SYNC_B	DU1_DB7	AUDIO_CLKOUT_C				GP4_25	GP4_25
	37	B4	SCL2_A		MSIOF1_SCK_B	DU1_DB6	AUDIO_CLKC_C	SSI_SCK4_B			GP4_24	GP4_24
	12	D6	MSIOF0_SS2_A		Reserved	DU1_DR7	Reserved	QSPI1_SSL			GP4_9	GP4_9
	16	AB11	DU0_DOTCLKOUT1	Reserved	MSIOF2_RXD_B				CS1#/A26		GP2_26	GP2_26
	18	AE3	EX_WAIT0	CAN_CLK_B	SCIF_CLK_A						GP1_22	GP1_22
	22	J1	SSI_SDATA2_A	HRTS1#_B					VI0_DATA4_VI0_B4		GP5_24	GP5_24
	32	Y1	D15	MSIOF2_SS2	PWM4_A		CAN1_TX_B	IRQ2	AVB_AVTP_MATCH_A		GP1_15	GP1_15
	36	Y22	USB0_PWEN								GP0_0	GP0_0
	38	AC5	QSPI0_IO3	RD#							GP1_20	GP1_20
	40	A3	SSI_SCK5_A			DU1_DOTCLKOUT1					GP5_0	GP5_0
	29	AB3	D4		IRQ3	TCLK1_A	PWM6_C	Reserved			GP1_4	GP1_4
	7	AE2	CLKOUT								GP0_4	GP0_4

Table 9: RZ/G1C CPU IOMUX for Expansion Connector2 Interfaces

Interface/ Function	Expansion Connnector2 Pin Numbers	RZ/G1C CPU Pin Number	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	GPIO	Default State
LVDS	7	AD17	TXOUT3P									TXOUT3P
	9	AE17	TXOUT3M									TXOUT3M
	13	AB16	TXCLKOUTP									TXCLKOUTP
	15	AC16	TXCLKOUTM									TXCLKOUTM
	19	AD15	TXOUT2P									TXOUT2P
	21	AE15	TXOUT2M									TXOUT2M
	25	AB14	TXOUT1P									TXOUT1P
	27	AC14	TXOUT1M									TXOUT1M
	31	AD13	TXOUT0P									TXOUT0P
	33	AE13	TXOUT0M									TXOUT0M
CAN0	16	B8	SD0_WP	IRQ7	CAN0_TX_A						GP0_12	GP0_12
	14	A8	SD0_CD		CAN0_RX_A						GP0_11	GP0_11
SSI1	1	A13	SD0_CLK			SSI_SCK1_C	RX3_C				GP0_5	GP0_5
	3	B13	SD0_DAT0			SSI_SDATA1_C	RX4_E				GP0_7	GP0_7
	5	D13	SD0_CMD			SSI_WS1_C	TX3_C				GP0_6	GP0_6
SSI0/9	6	D14	SD0_DAT1			SSI_SCK0129_B	TX4_E				GP0_8	GP0_8
	8	B14	SD0_DAT3			SSI_SDATA0_B	TX5_E				GP0_10	GP0_10
	10	C14	SD0_DAT2			SSI_WS0129_B	RX5_E				GP0_9	GP0_9
	12	D8	SD2_WP	SCIF3_SCK_A		DU1_DB3	SSI_SDATA9_B				GP4_21	GP4_21
SCIF5	28	AD2	D0	Reserved	SCL3_B	RX5_B	IRQ4	MSIOF2_RXD_C	SSI_SDATA5_B		GP1_0	GP1_0
	30	AD1	D1	Reserved	SDA3_B	TX5_B		MSIOF2_TXD_C	SSI_WS5_B		GP1_1	GP1_1
HSCIF1	32	E8	HCTS1#_A	PWM2_A		DU1_DG2	REMOCON_B				GP4_12	GP4_12
	34	D7	HRTS1#_A			DU1_DG3	SSI_WS1_B	IRQ1			GP4_13	GP4_13
	36	B7	HTX1_A	SDA4_A		DU1_DG1	TX0_A				GP4_11	GP4_11
	38	A7	HRX1_A	SCL4_A	PWM6_A	DU1_DG0	RX0_A				GP4_10	GP4_10

Interface/ Function	Expansion Connnector2 Pin Numbers	RZ/G1C CPU Pin Number	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	GPIO	Default State
HSCIF2	18	AA3	D8	HCTS2#	RX1_C	SCL1_D	PWM3_C				GP1_8	GP1_8
	20	AA2	D9	HRTS2#	TX1_C	SDA1_D					GP1_9	GP1_9
	22	AB2	D5	HRX2	SCL1_B	PWM2_C	TCLK2_B	Reserved			GP1_5	GP1_5
	24	AB1	D6	HTX2	SDA1_B	PWM4_C		Reserved			GP1_6	GP1_6
	26	AA4	D7	HSCK2	SCIF1_SCK_C	IRQ6	PWM5_C	Reserved			GP1_7	GP1_7
I2C3	37	A2	SSI_WS5_A		SCL3_C	DU1_DOTCLKIN					GP5_1	GP5_1
	39	B2	SSI_SDATA5_A		SDA3_C	DU1_DOTCLKOUT0					GP5_2	GP5_2
PWM0	40	H4	SSI_SDATA0_A	MSIOF1_SYNC_A	PWM0_C				VI0_R0		GP5_11	GP5_11

Table 10: RZ/G1C CPU IOMUX for Expansion Connector3 Interfaces

Interface/ Function	Expansion Connnector3 Pin Numbers	RZ/G1C CPU Pin Number	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	GPIO	Default State
SCIF1	17	F4	SSI_SDATA8_A	RX1_B			CAN0_RX_D	AVB_AVTP_CAPTURE_B	VI0_R7		GP5_19	GP5_19
	19	H1	SSI_WS1_A	TX1_B			CAN0_TX_D	AVB_AVTP_MATCH_B	VI0_DATA0_VI0_B0		GP5_20	GP5_20
SCIF4	18	AC2	D2	Reserved	RX4_B	SCL0_D	PWM1_C	MSIOF2_SCK_C	SSI_SCK5_B		GP1_2	GP1_2
	20	AC1	D3	Reserved	TX4_B	SDA0_D	PWM0_A	MSIOF2_SYNC_C			GP1_3	GP1_3
VI0	1	H2	SSI_SCK1_A	SCIF1_SCK_B	PWM1_D	IRQ9	REMOCON_A	DACK2	VI0_CLK	AVB_COL	GP5_18	GP5_18
	2	E4	AUDIO_CLKC_A	SCL4_B	Reserved				VI0_HSYNC#		GP5_30	GP5_30
	3	E1	AUDIO_CLKOUT_A	SDA4_B	Reserved				VI0_VSYNC#		GP5_31	GP5_31
	4	E2	AUDIO_CLKA_A	SCL0_B	Reserved	TANS1			VI0_CLKENB		GP5_28	GP5_28
	8	A6	MSIOF0_RXD_A	RX5_A	SCL2_C	DU1_DR2		QSPI1_MOSI/QSPI1_IO0	SSI_SDATA6_B	VI0_G2	GP4_4	GP4_4
	9	A5	MSIOF0_SCK_A	IRQ0	Reserved	DU1_DR4	Reserved	QSPI1_SPCLK	SSI_SCK78_B	VI0_G4	GP4_6	GP4_6
	10	B6	MSIOF0_TXD_A	TX5_A	SDA2_C	DU1_DR3		QSPI1_MISO/QSPI1_IO1	SSI_WS78_B	VI0_G3	GP4_5	GP4_5
	11	G1	SSI_WS0129_A	MSIOF1_TXD_A	TX5_D				VI0_G7		GP5_10	GP5_10
	12	C5	SCL1_A	RX4_A	PWM5_D	DU1_DR0			SSI_SCK6_B	VI0_G0	GP4_2	GP4_2
	13	D5	SDA1_A	TX4_A		DU1_DR1			SSI_WS6_B	VI0_G1	GP4_3	GP4_3
	14	F5	SSI_SDATA7_A			IRQ8	AUDIO_CLKA_D	CAN_CLK_D	VI0_G5		GP5_8	GP5_8
	16	G2	SSI_SCK0129_A	MSIOF1_RXD_A	RX5_D				VI0_G6		GP5_9	GP5_9
PWM2	7	K1	SSI_SDATA9_A	SCIF2_SCK_B	PWM2_D				VI0_DATA7_VI0_B7		GP5_27	GP5_27

3. TECHNICAL SPECIFICATION

This section provides detailed information about the RZ/G1C SBC technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The RZ/G1C SBC is designed to work with a +5V external power and uses on board voltage regulator for internal power management. 5V power input from an external power supply is connected to the SBC through Power Jack (J9). This 1.3mm x 3.9mm barrel connector Jack should fit DC Plugs with an inner dimension of 1.3mm and an outer dimension of 3.4mm. This Power Jack (J9) is physically located at the top of the SBC as shown below.

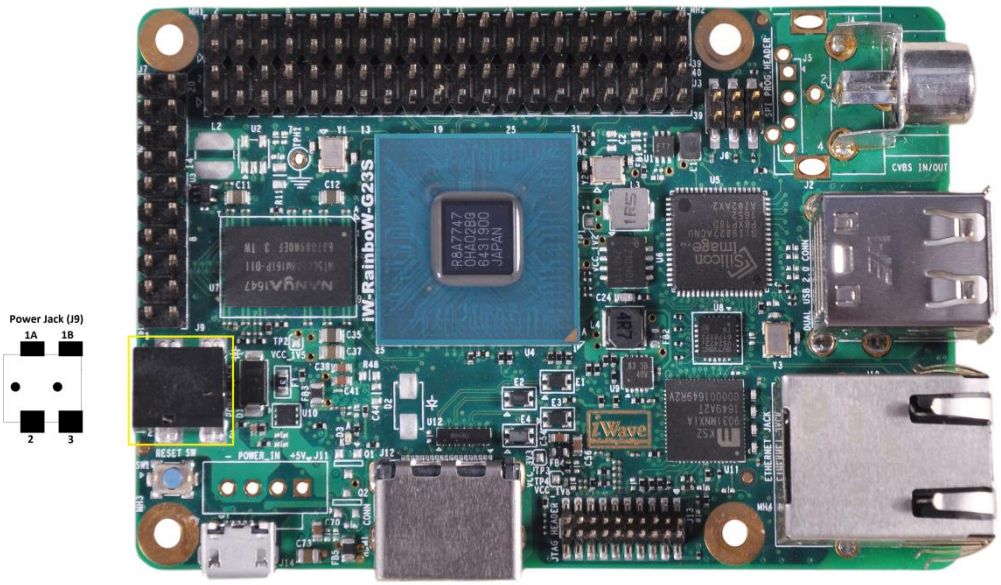


Figure 15: Power IN Connector

The below table provides the Power Input Requirement of RZ/G1C SBC.

Table 11: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_5V	4.75V	5V	5.25V	±50mV

3.1.2 Power Output Specification

The RZ/G1C SBC shares the on board +5V and +3.3V power to Expansion connectors for Add-On Module power.

Table 12: Power Output Specification

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Output Current (mA)
Power Output on Expansion Connector1					
1	VCC_5V	4.75V	5V	5.25V	1A[1]
2	VCC_3V3	3.1V	3.3V	3.5V	1A
Power Output on Expansion Connector2					
1	VCC_5V	4.75V	5V	5.25V	0.5A[1]
2	VCC_3V3	3.1V	3.3V	3.5V	0.5A
Power Output on Expansion Connector3					
1	VCC_5V	4.75V	5V	5.25V	0.5A[1]

[1] Maximum current value is provided based on the current carrying capacity of the Expansion connector pins. But actual maximum current value depends upon the external power supply capacity.

3.1.3 Power Consumption

Table 13: Power Consumption[1]

Task/Status	Power Rail	Current Drawn/Power Consumption
Run Mode Power Consumption		
EtherAVB 1000Mbps ping	VCC_5V	0.51A/2.55W
File transfer between USB Host, eMMC and Micro SD	VCC_5V	0.54A/2.7W
3D Gaming bench mark application on HDMI	VCC_5V	0.56A/2.8W
Dhrystone benchmark application	VCC_5V	0.57A/2.85W
CVBS video input capture	VCC_5V	0.58A/2.9W
1080p video playback on HDMI	VCC_5V	0.66A/3.3W
Typical Maximum Power: • 1080p video playback on HDMI • EtherAVB 1000Mbps ping • CVBS video input capture • File transfer between USB Host, eMMC and Micro SD • Dhrystone benchmark application • 3D Gaming bench mark application on HDMI	VCC_5V	0.76A/3.8W
Low Power Mode Power Consumption		
TBD	TBD	TBD

[1] Power consumption measurements have been done in iWave's RZ/G1C CPU based SBC (iW-G23S-CC02-3D512M-E008G-LEE) with iWave's Linux3.10.31 BSP (iW-PRFCC-SC-01-R3.0-REL1.0-Linux3.10.31)

3.2 Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of RZ/G1C SBC.

Table 14: Environmental Specification

Parameters	Min	Max
Operating temperature range[1,2]	-20°C	+85°C
Humidity - Operating	-	95%RH

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

[2] If CVBS Input RCA Jack is not supported in RZ/G1C SBC, then operating temperature range is -25°C to 85°C.

3.2.2 RoHS Compliance

iWave's RZ/G1C SBC is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.3 Electrostatic Discharge

iWave's RZ/G1C SBC is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SBC except at an electrostatic free workstation.

3.3 Mechanical Characteristics

3.3.1 RZ/G1C SBC Mechanical Dimensions

RZ/G1C SBC PCB size is 85mm x 56mm x 1.6mm. SBC mechanical dimension is shown below.

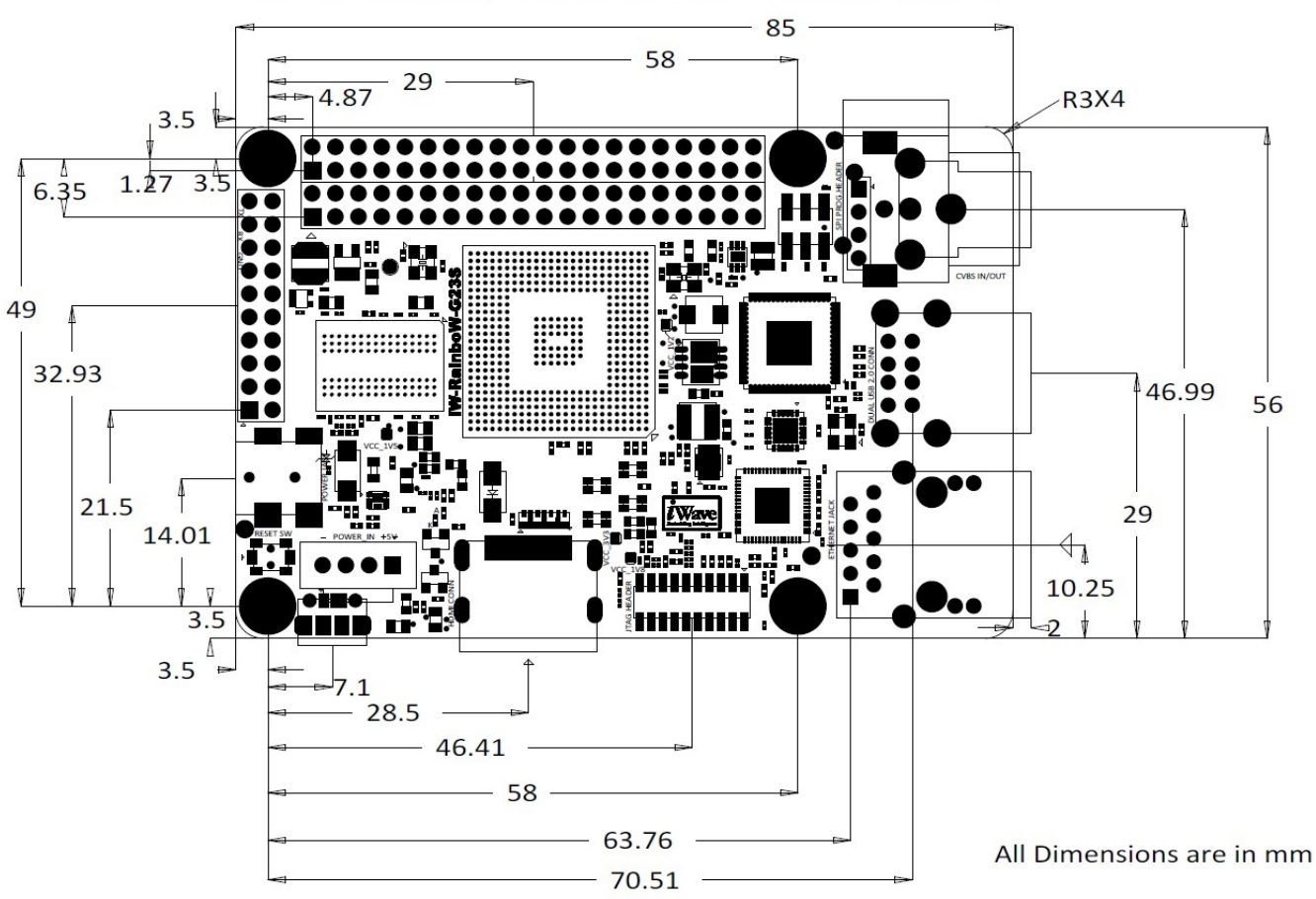


Figure 16: Mechanical Dimension of RZ/G1C SBC - Top View

RZ/G1C SBC PCB thickness is 1.6mm±0.1mm, top side maximum height connector is Dual USB Stack connector (15.97mm) followed by Ethernet connector (14.37mm) and bottom side maximum height component is Inductor (4.50mm) followed by Bulk Capacitor (2.5mm). Please refer the below figure for height details of the RZ/G1C SBC.

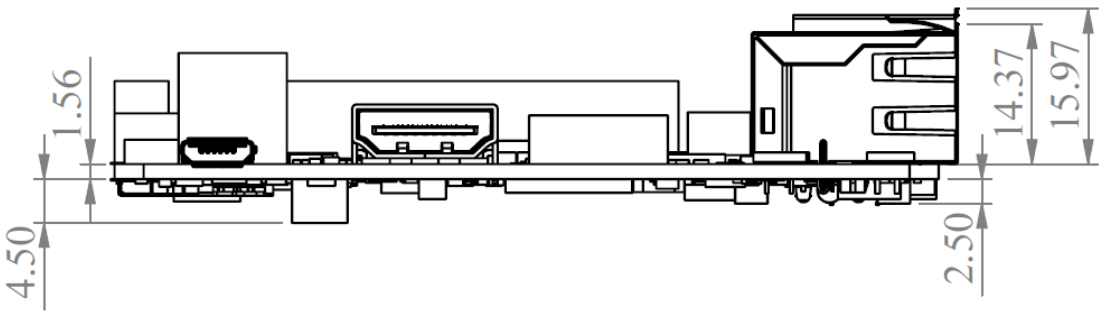


Figure 17: Mechanical Dimension of RZ/G1C SBC- Side View

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different RZ/G1C SBC variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SBC configurations. Also if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 15: Orderable Product Part Numbers

Product Part Number	Description	Temperature
RZ/G1C Dual Core CPU based SBC		
iW-G23S-CC02-3D512M-E008G-LEE	With RZ/G1C Dual Core PF CPU, 512MB RAM, 8GB eMMC with three Expansion connectors - Linux	Extended
iW-G23S-CC02-3D512M-E008G-LEE	With RZ/G1C Dual Core PF CPU, 512MB RAM, 8GB eMMC with three Expansion connectors – Boot code	Extended
RZ/G1C Solo Core CPU based SBC		
iW-G23S-CC01-3D512M-E008G-LEE	With RZ/G1C Solo Core PF CPU, 512MB RAM, 8GB eMMC with three Expansion connectors - Linux	Extended
iW-G23S-CC01-3D512M-E008G-LEE	With RZ/G1C Solo Core PF CPU, 512MB RAM, 8GB eMMC with three Expansion connectors – Boot code	Extended

Important Note: Some of the above-mentioned Part Number is subject to MOQ purchase. Please contact iWave for further details.

Note: For SBC identification purpose, Product Part Number and SBC Unique Serial Number are pasted as Label with Barcode readable format on SBC.


iWave
Embedding Intelligence